INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR
Department of Electronics and Electrical Communication Engineering

Code: EC31004 **Subject: VLSI ENGINEERING** **Exam: MID SEMESTER** **FEBRUARY 2018**

TIME : 2 HOURS **Total marks: 60**

Note: Assume suitable data (if necessary) and write all the assumptions clearly. All the questions are compulsory.

1. a. If a CMOS 90 nm NAND gate is driving a load capacitance of 900 fF while the propagation delay is 2.5 ns, what is the energy delay product?
b. What is latch-up in CMOS circuits? Draw the cross-section of a CMOS inverter and show an equivalent circuit that causes a latch-up.
c. Explain channel length modulation and velocity saturation in MOSFETs. How do they affect a MOSFET performance at certain operating conditions? Are they different for NMOS and PMOS transistors.

[3+6+6 marks]

2. a. Consider a digital circuit that has been fabricated by using a 350 nm fabrication process technology. Calculate the noise margin parameters if V_{IH}=2.5V, V_{IL}=0.5 V, V_{OH}= 3.2 V, and V_{OL}=0.1 V,.
b. A transient (or time domain) digital signal takes 5 ns for 0 V to 5 V, and 7 ns for 5V to 0V transitions. Calculate the rise time and the fall time.

[3+2 marks]

3. Draw, label and explain (briefly, with sufficient clarity) the process steps that are involved in VLSI fabrication of a CMOS inverter on an n-type silicon wafer by using a single tub technology. How may masks are required? Show their relative shapes.

[10+1+4 marks]

4. Draw and label the process steps for VLSI fabrication of an silicon on insulator (SOI) n-channel MOSFET. Explain the steps in brief. State the advantages and disadvantages of SOI technology over standard CMOS technology. Mention two common applications of the SOI MOSFETs.

[6+3+1 marks]

5. Draw and explain the ion implantation set-up/ equipment. Explain the roles of dose and energy in ion implantation technique.

[3+2 marks]

6. State true/false. If the statement is false, identify the mistake and write the correct statement/phase/word:

[5 marks]

a. Design rules in VLSI engineering are the design guidelines that are specified *only* for MOSFETs.
b. Source or drain regions of a MOSFET is fabricated by using ion implantation.
c. Poly-silicon is also commonly known as a single crystal silicon.
d. Silicon nitride (Si_3N_4) offers lower dielectric constant as compared to silicon dioxide (SiO_2).
e. In positive photo resists, the areas where the light strikes become polymerized and more difficult to dissolve in solvents.

f. Photolithography uses infra-red light for exposure of photo resist.
g. Metal (eg. Au) deposition on a semiconductor wafer is typically accomplished by means rapid thermal annealing.
h. Flip-chip bonding is more space efficient than wire bonding.
i. The 180 nm process technology based VLSI chips have the width (W) as 180 nm.
j. Bipolar VLSI circuits are slower than CMOS equivalent.

7. Fill-in the blanks:

[5 marks]

a. CVD process utilizes _____ and _____ gases.
b. PVD is abbreviated as _____.
c. FCBGA is abbreviated as _____.
d. Mobility of electrons is_____.
e. Metals or _____ is used as gate contact.
f. Crosstalk in SOI MOSFETs is _____ as compared to single-tub MOSFETs, in a given process technology node (eg. 45 nm).
g. The fan-in of a 4 input AND gate is _____.
h. Chemical formula of silane is _____.
i. The pitch of a dual in-line package (DIP) chip carrier is _____.
j. A 3D packaging of VLSI chips are beneficial for saving _____.

END OF QUESTION PAPER
