Indian Institute of Technology Kharagpur

SPRING Semester, 2012

COMPUTER SCIENCE AND ENGINEERING

CS21002: Switching Circuits and Logic Design

Mid–semester Examination

Full Marks: 60

Time allowed: 2 hours

INSTRUCTIONS: Special credit would be given for answers which are short and to–the–point. Illegible handwriting would be penalized. ANSWER ALL QUESTIONS.

1. This question is on manipulation of Boolean algebraic expressions, and CMOS circuits. For parts (a) and (b), use identities of Boolean algebra.

(a) Prove that the switching expression $T(x,y,z) = (x+y)\left[x'(y'+z')\right]' + x'y' + x'z'$ is a tautology. (5 marks)

(b) You are supplied with just one NOT gate and an unlimited number of AND and OR gates. Implement the switching function $T(w,x,y,z) = w'x + x'y + xz'$ using these gates (draw the gate–level diagram). Only non-complemented variables are available as inputs. (5 marks)

(c) You have been supplied with only NAND2 and NAND3 gates. Implement the following function (draw the gate–level diagram): $f(w,x,y,z) = w(x+y+z) + xyz$. Assume only the non–complemented variables are available as inputs. (5 marks)

(d) A CMOS inverter has $\tau_{PLH} = 1.5$ns and $\tau_{PHL} = 1.0$ns. Calculate the maximum frequency that would be available from a ring oscillator comprised of such inverters. (2 marks)

(e) An inexperienced designer was asked to design a CMOS inverter. By mistake, he swapped the positions of the PMOS and the NMOS transistors, i.e. he designed the inverter with the PMOS drain connected to ground and the NMOS drain connected to V_{DD}. He then applied a 0–5 volt square wave at the input of the inverter and observed the output voltage waveform on an oscilloscope. Draw the output voltage waveform against the input waveform as observed by the designer. Assume $V_{tn} = 1$V, $|V_{tp}| = 1V$, $V_{DD} = 5$V. Ignore any propagation delay, and *body effect*, i.e. the variation of threshold voltage with change in V_{BS}. (3 marks)

2. This question is on two–level logic minimization.

(a) Is an irredundant SoP expression of a Boolean function always minimal? If yes, give justifications. If not, give an example in support of your answer. (5 marks)

(b) Minimize the Boolean function $f(A,B,C,D) = \Sigma(1,2,3,5,6,7,8,9,12,13,15)$ using the *Quine-McCluskey* procedure. (12 marks)

(c) Give the *zero–one integer linear programme* formulation of the *prime implicant chart covering* step of the *Quine-McCluskey* procedure. (5 marks)

3. This question is on combinational circuit building blocks.

(a) For addition and subtraction in the 2's complement system, what is the nature of the operand values for which overflow is possible? Give Boolean algebraic justification in support of your answer, assuming a ripple–carry implementation of a n–bit adder. (*Hints*: Think about the different possible logic expressions for the carry of a full adder that you have studied. Select the appropriate logic expression, and then manipulate the expression of the *overflow* bit.) (6 marks)

(b) Implement the following Boolean function using a 8:1 multiplexer: $f(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 15)$. (4 marks)

(c) Consider a 3–input gate whose output is given by $T(A, B, C) = \Sigma(3, 5, 6)$.

(i) Prove that T gates plus the logic value 1 are functionally complete. (2 marks)

(ii) Realize, by means of two T gates (and no extra gate), the function $f(w, x, y, z) = \Sigma(0, 1, 2, 4, 7, 8, 9, 10, 12, 15)$. (6 marks)