INDIAN INSTITUTE OF TECHNOLOGY

Date: **17 Feb 2012**, FN/AN, Time: **2 Hrs.**, Full Marks: **30**, Dept. : **ECE**, No. of Students : **103**
3rd Yr. B.Tech (H), **Mid Spring** Semester, Sub. No.: **EC31004**, Sub. Name: **VLSI Engineering**

Instruction:

- All diagrams must be neatly drawn and clearly labeled. Answers must be brief and to the point.
- The final answers (numerical values with unit) should be underlined or enclosed within box with unit.
- For every Question No., start your answer from a new page.
  Avoid writing answers of the various parts of a single question at different locations in your answer-script.
- For any value related to any device parameter or circuit parameter, which you may find not given with a problem, either assume a suitable value for such parameter or express the final answer in terms of that parameter.

Q 1. 10 Marks = 5 x (0.5 + 1.5) marks

For all questions in (**Q 1**), select the correct combinations of the options to make the following statements correct. For every statement provide brief reasoning or calculation (using diagrams, if relevant).

(1.A) [Carrier velocity saturation / Drain Induced Barrier Lowering (DIBL)] [increases / reduces] the average value of V_{Tn} of an NMOS transistor.

(1.B) [Local oxidation of Silicon (LOCOS) / Shallow Trench Isolation (STI)] gives rise to bird's beak formation for the [gate-oxide / field-oxide / inter-metal-layer oxide].

(1.C) [Constant-field / constant-voltage] scaling [increases / lowers] the power-dissipation per unit-area value by a factor of [S^2 / S / S^{-1}], where scaling factor = S, S > 1. → S^3

(1.D) For a self-aligned gate NMOS transistor, the [n-well diffusion / p-well diffusion / Drain diffusion] is done later than [poly-Si / inter-metal-layer oxide / metal-1 layer] deposition.

(1.E) For some 90 nm 1V process, punch-through break-down of the channel of a PMOS transistor (when it is OFF) can happen at a relatively [lower / higher] V_{SD} for a W-L value of [180nm-180nm / 1800nm-180nm / 180nm-90nm].

(1.F) [bonus point] Thermal-noise in the MOSFET-channel will [lower / increase] the value of the input [signal sensitivity / signal handling capacity / signal bandwidth] for an MOS driver transistor in an amplifier circuit.

(1.G) [bonus point] Implanting the substrate with dopant atoms underneath the gate-oxide (i.e. channel implantation) of a transistor can be used as a technique for altering the threshold voltage of a transistor. Therefore, for [an enhancement / a depletion] type NMOS transistor, a p-type channel-implantation should be used to realize a [negative / positive] V_{Tn} value.

Q 2. 6 Marks = 3 x (1 + 1) marks

For the Figure 1, show the vertical cross-sectional view along the dotted line A-A' of the photolithography masks and the horizontal cross-sectional view (top-view) of the photolithography masks for [assuming positive photoresist]:

(2.A) Poly-Si Gate **(2.B)** NMOS Drain-Source **(2.C)** Metal-1 interconnects

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Q 3. 14 Marks = 7 x 2 marks

Consider the physical design of the circuit in Figure 1. Grid-size shown in the adjacent ruler = 2 x (Design-rule λ)
Minimum channel length: 250 nm = 2 x (Design-rule λ). C_{OX} = 5 fF / um^2; k_n' = 100 uA/V^2, k_p' = 40 uA/V^2; $V_{Tn} = -V_{Tp}$ = 500 mv; Channel length modulation param: $\lambda_n = \lambda_p$ = 0.05 V^{-1}; Carrier velocity saturation: E_{crit}= 2 V/um, $v_{sat} = 10^5$ m/s
Drain/Source-to-well/bulk bottom-wall junction capacitance for NMOS and PMOS: C_{j0} =2 fF/um^2, m_j =0.5, ϕ_0 = 1 V
Drain/Source-to-well/bulk side-wall junction capacitance: C_{jsw0} = 0.2 fF/um, m_{jsw} = 0.3, ϕ_{0sw} = 1 V
Overlap capacitance parameters for NMOS and PMOS: $C_{GBO} = C_{GDO} = C_{GSO}$ = 0.2 fF/um, G-to-bulk/well/D/S overlap = 25 nm
Assume long-channel drain-current behavior for the MOSFETs unless specifically mentioned.

(3.A) Draw the complete circuit (schematic) diagram. Include in the diagram all the parasitic capacitances between various circuit nodes, which are originating from the transistors. [2]

(3.B) Calculate the DC bias current (I_{DC}) and the DC bias voltage of V_{OUT}. [1+1]

(3.C) Find the expression for the mid-frequency gain (A_{v0})[in terms of device geometry values, bias-current, R_{GD}] and calculate its value. [1+1]

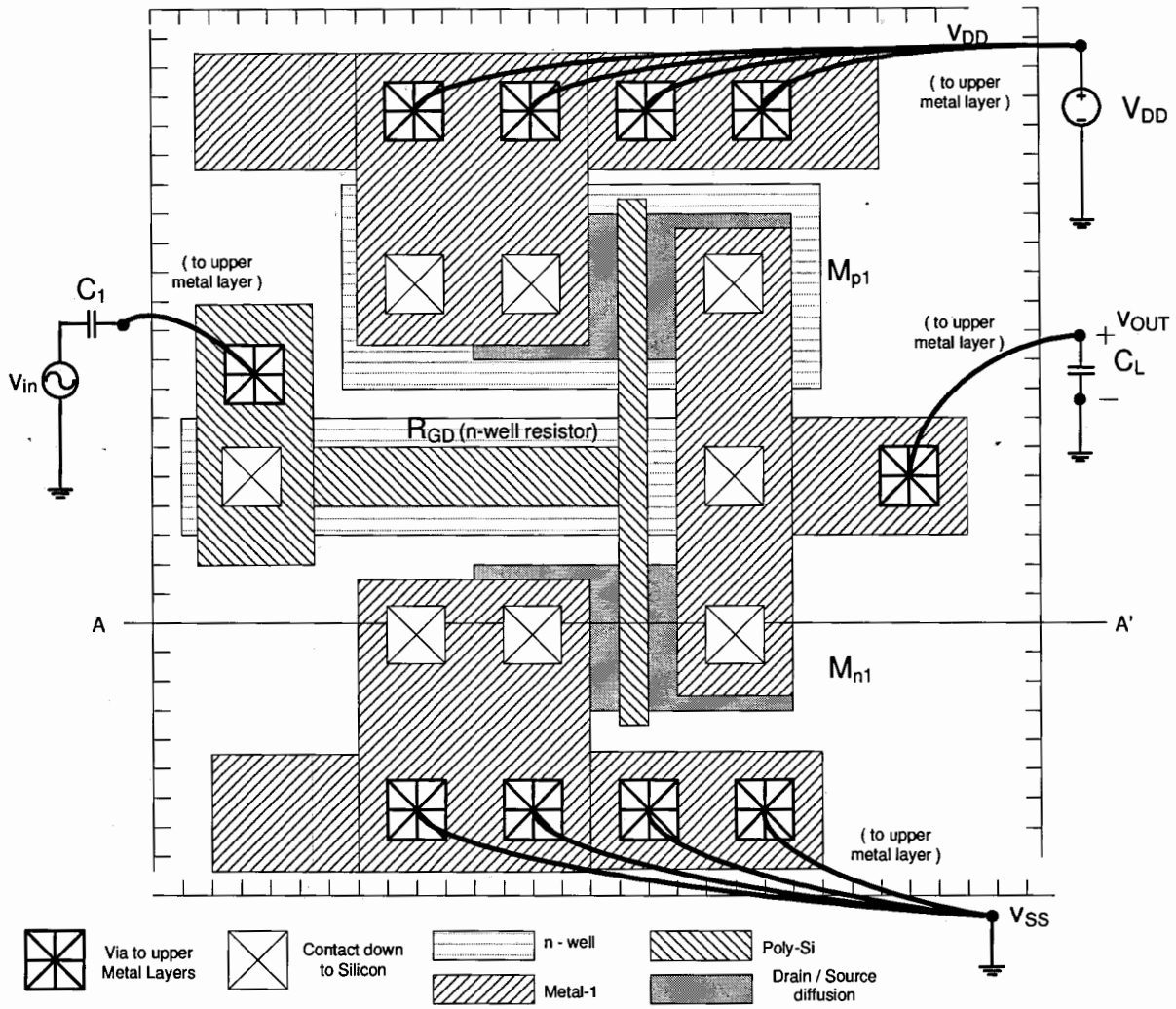
(3.D) Find the expression for output signal handling capacity [in peak-to-peak v_{out}] and calculate its value. [1+1]

(3.E) Find the value of the equivalent parasitic input-capacitance C_{in} (between the common gate-terminal and ac-GND) at mid-frequency which is originating from the transistor layout. [2]

(3.F) Find the value of the equivalent parasitic output capacitance C_{out} (between the common drain terminal and ac-GND) at mid-frequency, which is originating from the transistor layout [2]

(3.G) Find the expression for unity-gain frequency (ω_T) in terms of device geometry values, bias-current, R_{GD}, load C_L and effective parasitic C_{in} and C_{out} at that frequency. Calculate the value of ω_T [radian/s]. [1+1]

(3.H) [Bonus point] Now assume carrier-velocity saturation through the MOSFETs. Calculate I_{DC} and DC value of V_{OUT}. Calculate the value of ω_T. [2+2]



Circuit parameters: C_1 = 1 uF, C_L = 100 fF, V_{DD} = 2.5V, R_{GD} = 100 KΩ, $(W/L)_n = (W/L)_p = 10\lambda/2\lambda$, v_{in}=100 mV(pk-pk)

Figure 1: Physical design of an amplifier in an IC.

You may or may not find the following equations useful.

Voltage invariant p-n junction capacitance averaging factor (for a voltage swing between V_{low} and V_{high}),

$$K_{m,\emptyset_0}(V_{low}, V_{high}) = \frac{\emptyset_0}{(1-m)(V_{high}-V_{low})}\left[\left(1+\frac{V_{high}}{\emptyset_0}\right)^{(1-m)} - \left(1+\frac{V_{low}}{\emptyset_0}\right)^{(1-m)}\right]$$

Charge-carrier velocity under applied field: $v_{n,p} = \mu_{n,p}E/\left(1+\frac{E}{E_{crit}}\right), for\ E \le E_{crit}\ and\ v_{n,p} = v_{sat}, for\ E \ge E_{crit}$

Transistor drain-current under charge-carrier velocity saturation, $I_D \approx$

$$\begin{cases} C_{OX}W\left[(V_{GS}-V_{Tn}) - V_{DS,SAT}\right]v_{sat}, for\ V_{GS} > V_{Tn}, V_{DS} \ge V_{DS,SAT}, V_{DS,SAT} = \dfrac{(V_{GS}-V_{Tn})}{1+\dfrac{(V_{GS}-V_{Tn})}{E_{crit}L}} \\ \dfrac{\mu_n C_{OX}\left(\frac{W}{L}\right)\left[(V_{GS}-V_{Tn})V_{DS} - \frac{V_{DS}^2}{2}\right]}{1+\frac{V_{DS}}{E_{crit}L}}, for\ V_{GS} > V_{Tn}, V_{DS} < V_{DS,SAT} \end{cases}$$