Indian Institute of Technology, Kharagpur -721302

End-Semester

Time: 3 hours; Full Marks: 50; Number of Students 182

Spring Semester, 2010; Department: E & ECE; Subject code EC 21008

II year B. Tech.; Subject name: **Analog Electronic Circuits**

Instruction: Answer ***ALL*** questions and **strictly in the same order** of the questions.

Where ever it is necessary, you may use assumption(s) with reasonable justification

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Given: (i) Default values of parameters for MOST, $|V_{th}| = 1.0\text{V}$ and $\lambda \approx 0\ \text{V}^{-1}$

(ii) Default values of parameters related to BJT,

$$V_T = 26\text{mV};\ |V_{BE(on)}| \approx 0.6\text{V} \quad \text{and} \quad |V_{CE(sat)}| \approx 0.3\text{V}$$

Q.1. (a) Draw the circuit diagram of a single stage amplifier using BJT that utilizes current-series feedback. Express its feedback factor β in terms of the circuit component values. Write down (derivation not required) the expression for its input resistance in terms of β, appropriate gain parameter and its original input resistance.

(3+1+1)

(b) Draw the circuit diagram of a single stage amplifier using BJT that utilizes voltage-shunt feedback. Express its feedback factor β in terms of the circuit component values. Write down (derivation not required) the expression for its input resistance in terms of β, appropriate gain parameter and its original input resistance before the application of feedback.

(3+1+1)

Q.2. (a) Neglecting $V_{CE(sat)}$, calculate the numerical value for the maximum possible power efficiency of a Class A amplifier with the following biasing conditions: $V_{CE} = 0.5\ V_{CC}$, the voltage drop across the collector resistor (which is also serving as the load) is 40% of V_{CC} and the voltage drop across the emitter resistor (which is bypassed with the help of a very large capacitor) is 10% of V_{CC}. What is the upper bound (derivation not required) of power efficiency for a transformer coupled Class A amplifier?

(4+1)

(b) Draw the circuit diagram of an ideal Class B push pull amplifier. Derive the maximum possible efficiency of an ideal Class B amplifier neglecting $V_{CE(sat)}$ and V_γ (cut-in voltage) of the B-E junction diode.

(2+3)

Q.3.

(a) Mention the model parameters (of a BJT or of a MOSFET, as appropriate) that the following expressions do represent (symbols are having their usual significance).:

(i) V_T/I_B, (ii) V_A/I_C, (iii) I_C/V_T,

(iv) $V_{GS} - \sqrt{(I_D/K)}$, (v) $1/(\lambda I_D)$.

(5)

Q.3. (b) (i) Calculate overall small signal gain of the circuit given in Fig.1 in mid – frequency range. (**Given** $K = 250\ \mu A / V^2$)

(3)

(ii) Swap the two stages and calculate the overall gain in mid – frequency range.

(2)

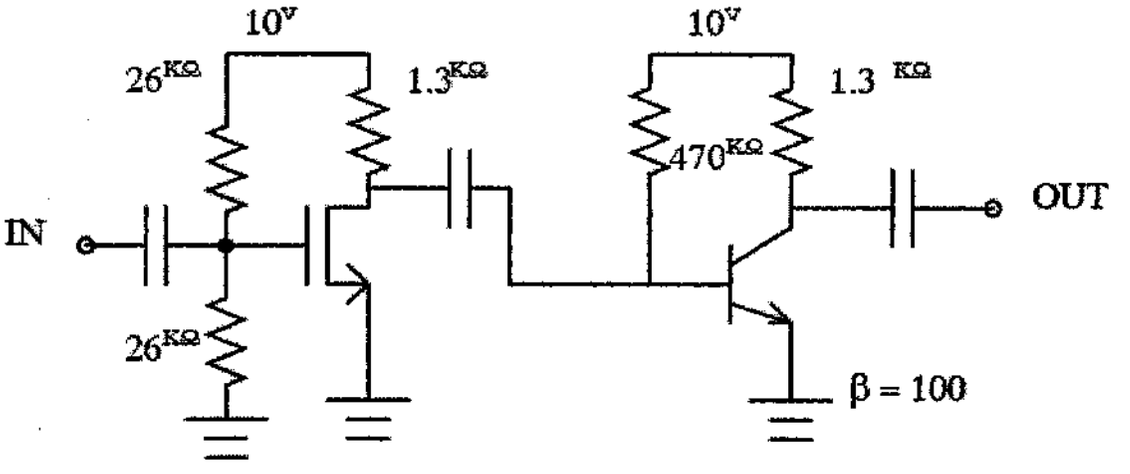

Fig. -1

Q.4. (a) In a series-shunt (voltage mixing and voltage sampling) negative feedback system, forward amplifier has 52dB low frequency voltage gain. The amplifier has two poles, one at 10 kHz and the other one at 1MHz. In the system, feedback circuit has an attenuation of 0.5. In terms of port impedance, assume that the feedback circuit is ideal one.

(i) Neatly sketch the Bode' plots of the forward amplifier and the loop gain of the system.

(ii) Calculate the frequency at which the loop gain of the system becomes unity.

(iii) Calculate the phase margin of the feedback system.

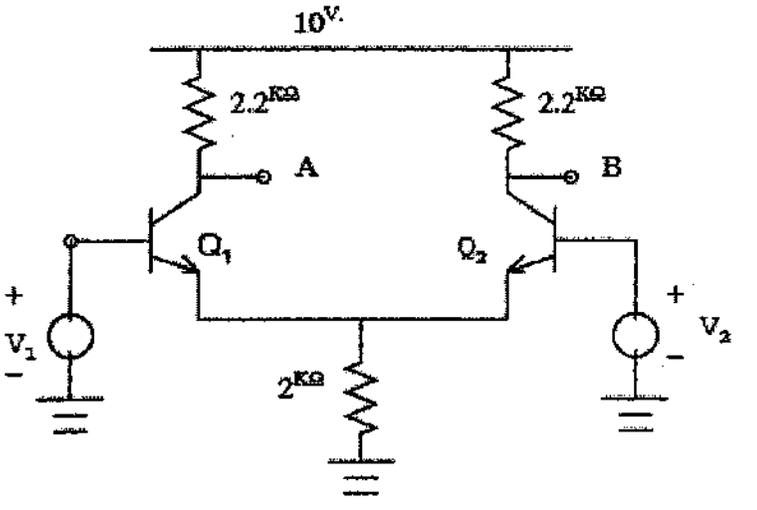

Fig. - 2

Q. 4. (b) A differential amplifier circuit is shown in Fig. 2

(i) Assuming Q_1 and Q_2 are identical transistors and their V_A's are very high, calculate the values of small signal differential mode gain and common mode gain of the amplifier with a d.c. level of V_1 and V_2 equal to 3.6V.

(ii) Now, Q_2 is replaced by a transistor Q_3 whose characteristic has a small mismatch with respect to that of Q_1. Due to this mismatch, with a 3.6V d.c. level of V_1 and V_2, the observed voltage at nodes A and B are 8.2V and 5.2V respectively. While maintaining V_2 at 3.6V, what should be the voltage at V_1 so that $V_A = V_B$?

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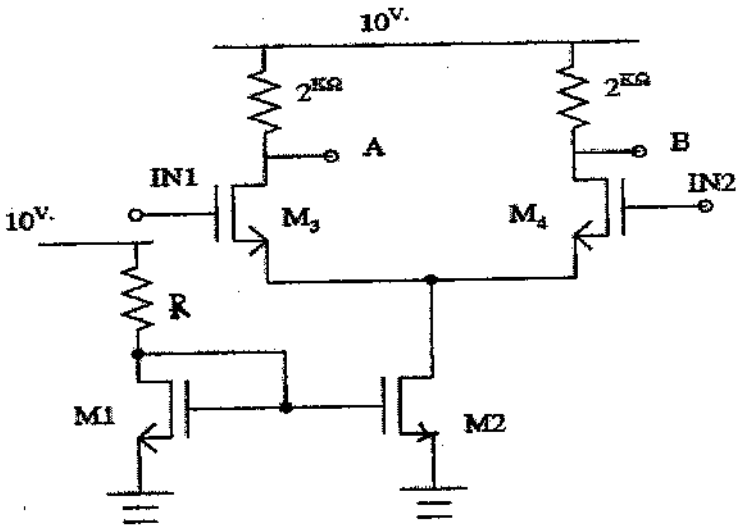

Fig. - 3

Q.5. Refer to the differential amplifier circuit in Fig. 3.

Given: values of transconductance factors of different transistors are,
M1 = 0.5 mA/V^2, M2 = 2 mA/V^2, M3, M4 = 4 mA / V^2

(i) What is the value of R so that the tail current of the differential amplifier is 4 mA

(ii) What is the minimum input common mode level so that all transistors are in saturation region?

(iii)For 5V input common mode level, draw small signal equivalent circuit of the amplifier

(iv)Calculate small signal differential mode gain of the circuit for,
$V_{in1} = 5 + 0.1$ Sin (4000πt) Volts and $V_{in2} = 5$ Volts.

(v) For the input voltages as mentioned in part (iv), neatly draw the voltage waveforms at node 'B' and at the source node of M3 (and M4).

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