INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

Date ..... – 02 – 2011..... FN / AN Time : 2 / ~~3~~ Hrs. Full Marks ....30..... No. of Students ..... 85 .....

~~Autumn~~ / Spring Semester ..... Dept. ..... **E & ECE** ..... Sub. No. ..... **EC 31004** .....

... 3rd .... Yr. B. Tech. (H) / ~~B. Arch (H)~~ / ~~M. Sc.~~ Sub. Name ..... **VLSI Engineering** .....

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The formulas (given only for NMOS device), which you may or may not need for the problems, are given below:

- Dielectric constant: $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m, ε_r of $SiO_2 = 3.9$
- $\beta_n = k_n' \left(\frac{W}{L}\right)_n = \mu_n C_{OX} \left(\frac{W}{L}\right)_n$
- Drain current:
  - $I_{Dn} = 0$, when $(V_{GSn} - V_{Tn}) < 0$
  - $I_{Dn} = \frac{\beta_n}{2}[2(V_{GSn} - V_{Tn}) - V_{DSn}] \cdot V_{DSn}$, when $(V_{GSn} - V_{Tn}) \geq 0$ and $V_{DSn} < V_{DSn,SAT}$
  - $I_{Dn} = \frac{\beta_n}{2}[2(V_{GSn} - V_{Tn}) - V_{DSn,SAT}] \cdot V_{DSn,SAT} \cdot (1 + \lambda_n V_{DSn})$, when $(V_{GSn} - V_{Tn}) \geq 0$ and $V_{DSn} < V_{DSn,SAT}$

    $V_{DSn,SAT} = V_{GSn} - V_{Tn}$

For all the numerical problems use the following process parameters, unless specified otherwise for the individual problem: $V_{DD} = 3$ V, $k_n' = 100$ μA / V², $k_p' = 50$ μA / V², $V_{Tn} = 0.5$V, $V_{Tp} = -0.5$ V. Assume $\lambda_n = \lambda_p \approx 0$ V^{-1}

1. Problem on inverter circuit: (2 + 2 + 2) = 6 points

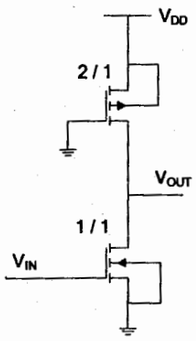

Figure 1. Inverter circuit

Refer to the inverter circuits in Figure 1.

Design parameters:
The NMOS and PMOS channel-width / channel-length ratios are as shown in the figure.

For the circuits shown:
Calculate logic-high output voltage level, V_{OH}
Calculate logic-low output voltage level, V_{OL}
Calculate the switching threshold voltage, V_I

2. Problem on FPGA based logic design: 6 points

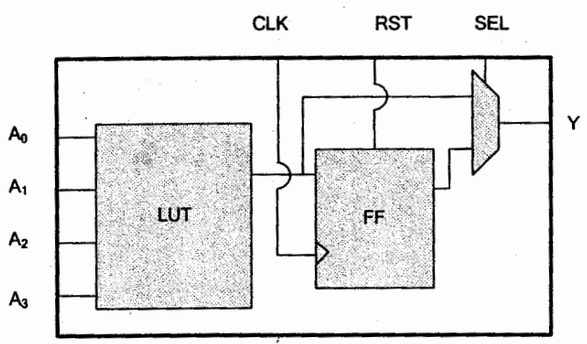

Figure 2. CLB for an FPGA

Figure 2 shows the configurable logic block of an FPGA. For the following Boolean function show the circuit connection:

At every positive-edge of CLK,

P[3:0] = Q[3:0] + 1;

Where, P and Q are 4-bit registers and '+' represents arithmetic addition of two unsigned numbers.

Show the entire circuit of FPGA realizing the above operation. (Ignore switch-matrix connection details in your circuit diagram).

3. Problem on CMOS Fabrication Process: 6 points

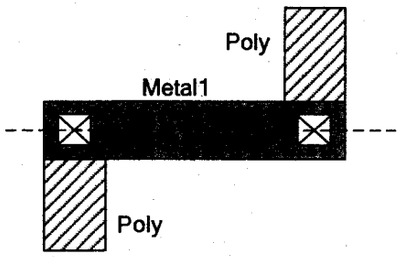

Figure 3. Metal1 pattern over Poly-Si pattern

Consider a CMOS fabrication process. Refer to Figure 3, where the physical design (layout) of a section of interconnection using Poly-Si and Metal1 layers is shown.

Using a sequence of diagrams along the cross-section (dotted line in Figure 3), show all the fabrication steps after the formation of Poly-Si layer up to the completion of Metal1 layer interconnects.

Show the photolithography mask cross-sections, wherever applicable.

4. Problem on circuit layout: (4+8) = 12 points

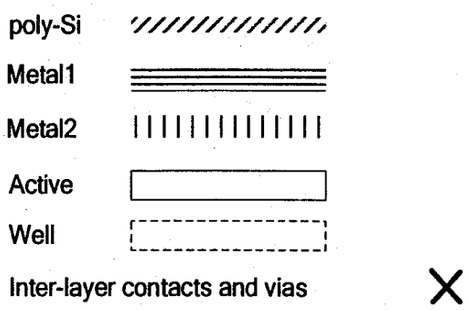

Figure 4. Stick-diagram symbols.

(i) The boolean function for carry-out bit of a full-adder is given by:
$C_{OUT} = f_1(A,B,C_{IN}) = AB + BC_{IN} + C_{IN}A$,
Draw the transistor-level circuit diagram, where no more than two transistors are in series in the pull-up network and in the pull-down network of the static CMOS logic.

(ii) Assuming standard-cell design, give the stick-diagram of step (i) for the cell, where the layout shares the drain/source areas of the nearest transistor, whenever allowed in standard-cell design. Mark all the circuit drain and source nodes in the diagram as $D(Mn_{CIN})$, $S(Mp_A)$, etc. and list down all the circuit nodes where drain/source sharing has been done.