INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

Date: 17 Feb 2012(AN) Time: 2 Hrs. Full Marks: 30 No. of Students: 251

Mid Spring Semester 2011-2012 Department: E&ECE Subject No.: EC 21008/EC21010

B. Tech. Subject Name: **ANALOG ELECTRONIC CIRCUITS**

Answer ALL the questions.

1. A signal generator generates 330 mV_{PP} signal under unloaded condition. The voltage drops down to 30 mV_{PP} when a load R_L is directly connected to the signal generator. When the same signal generator is connected to the input of an amplifier having an inherent voltage gain of 100, input resistance of 1 KΩ and output resistance of 225 Ω, the voltage observed across the same load R_L (which is now connected to the output of the amplifier), to be 4 V_{PP}. Write the expression of the overall voltage gain. Find out the probable values of the load resistance R_L and the source resistance r_s of the signal generator.

(6)

2. Design a common emitter amplifier (without emitter resistor) to maximize the output swing for an available power supply of 9 V, while maintaining a quiescent collector current of 3 mA. Assume $\beta = 100$, $V_{BE(ON)} = 0.6$ V. Ignore $V_{CE(SAT)}$ for this calculation. Set the lower cutoff frequency to be equal to 20 Hz. Draw the complete circuit along with the values of the associated components. Calculate the mid-frequency voltage gain of your designed circuit.

(6)

3. Draw the frequency response of a common source amplifier clearly indicating the numerical values of lower cutoff frequency, mid-frequency voltage gain and upper cutoff frequency, for the following given device parameters and operating conditions: $V_{th} = 1$ V, $K = 500\ \mu A/V^2$, $\lambda = 0$, $C_{gs} = 2$ pF, $C_{gd} = 2$ pF. Assume a power supply voltage of 6 V, gate voltage set at 3 V by a potential divider comprised of two 100 KΩ resistor connected between gate and power supply terminals. Source is directly connected to ground and drain is connected to the power supply through a fixed resistance such that the drain voltage is 4 V. The amplifier is driven by a signal source having a source resistance of 600 Ω connected to the gate terminal via a 1 μF capacitor.

(6)

4. Draw the circuit diagram of a common base amplifier including all the biasing arrangements from a single power supply. Clearly identify the input and the output terminals. Draw the small signal equivalent circuit and derive the expressions for its voltage gain and input resistance.

(6)

5. Draw the circuit diagram of an emitter follower using a p-n-p transistor. Draw he small signal equivalent circuit. Derive the expression for input resistance of the circuit. Derive the expression of output resistance of the emitter follower when it is driven by a signal source with nonzero source resistance.

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