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INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

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B. Tech Subject Name: Digital Electronic Circuits

Instructions: This question paper consists of **four** pages and six questions, each carrying 20 marks.. Answers to parts of one question must be written in one place. Otherwise, they will **not** be checked. Answer **any five** questions. Note carefully that **only** the **first five** answers will be checked even if you answer all six questions. All questions have been adequately explained and need no further clarification.

1 (a) Realize the following three switching functions by means of a 3-input 3-output **PROM** (programmable read-only memory), namely $P(a,b,c) = ab + \bar{b}c$; $Q(a,b,c) = (a+\bar{b}+c)(\bar{a}+b)$; and $R(a,b,c) = a + bc$. Note that a is the most significant variable. Draw the complete AND and OR arrays, showing clearly where the fuses (links) will remain after programming. [8]

(b) Draw the complete transistor diagram of a **bipolar** static RAM cell including the read amplifier, the write amplifier and the control logic circuit. Referring to your diagram, briefly explain how one can **read** from and **write** into the memory cell. [12]

2 (a) The state diagram of a synchronous sequential circuit with one input and one output is shown in Figure 1. Do **not** attempt any state reduction of the fsm (finite state machine). For the state assignment **A = 001**; **B = 010**; **C = 011**; **D = 100**; and **E = 101**, give a realization of the circuit using negative edge-triggered ***JK*** flip-flops. Write the excitation table of a *JK* flip-flop. Write the state transition table, the excitation table and the output table for the given circuit. Minimize the size of the required combinational logic. Draw the circuit diagram. [14]

(b) Show how a ***D*** flip-flop (FF) can be converted to a ***JK*** FF. That is, you have actually an *D* FF which will be made to behave like a *JK* FF with the addition of two external inputs *J* and *K* and a combinational circuit whose output is fed as an excitation input to the available *D* FF. Write the complete conversion table and design the combinational circuit with minimum size. Draw the logic diagram of the complete circuit. [6]

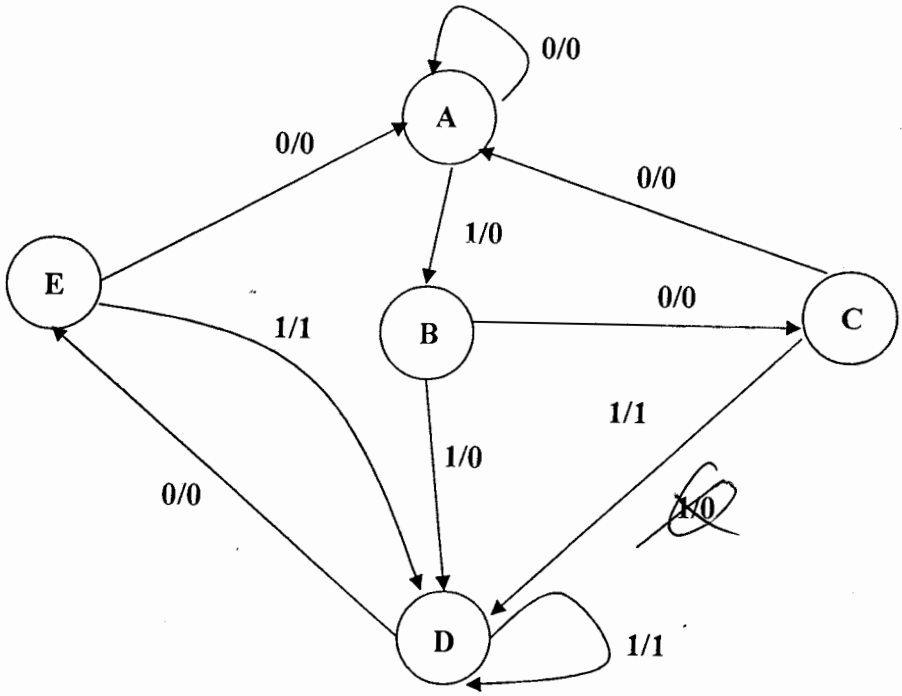

Figure 1: State diagram of a sequential circuit (Question 2(a))

3 (a) Consider a *fundamental mode* **asynchronous** sequential circuit with two level inputs A and B, and one output X. Whenever, A=0, X=0. The first change in the input B that occurs while A=1 will make the output become X=1. The X=1 output must not change to X=0 until A=0. A typical input-output sequence of the desired circuit is given as follows:

A: 0 0 1 1 1 0 0 0 1 1 1 0
B: 0 1 1 0 1 1 1 0 0 1 1 1
X: 0 0 0 1 1 0 0 0 0 1 1 0

Construct a **primitive flow table** for this circuit depicting all the **stable** and **unstable** states and outputs wherever it is possible to specify them. Explain all the stable states in terms of the inputs and the output. Next using the **implication table** technique, determine a reduced flow table from the primitive flow table. [4+5+6]

(b) Draw the complete transistor diagram of a 6-transistor **MOS static** memory cell. Briefly explain the **reading** and the **writing** operations of this cell. [5]

4 (a) Draw the complete circuit of a two-input TTL (transistor-transistor logic) **NOR** gate with a totem-pole configuration at the output stage. What role do the phase-splitter transistors play? Also explain the need of the diode in the pull-up element of the totem-pole output stage. [8]

(b) Define fan-out of a TTL gate. You are asked to find how many standard TTL 2-input NAND gates can be driven by an LS-TTL 2-input NAND gate. Given that for an LS-TTL 2-input NAND gate, the maximum vales of the currents are as follows: $I_{OH} = -400\,\mu A$; $I_{OL} = 8\ mA$; $I_{IH} = 20\,\mu A$ and $I_{IL} = -0.4\,mA$. Whereas, for a standard TTL 2-input NAND gate, the maximum vales of the currents are as follows: - $I_{OH} = -400\,\mu A$; $I_{OL} = 16\ mA$; $I_{IH} = 40\,\mu A$ and $I_{IL} = -1.6\,mA$. [4]

(c) Draw the circuit diagram for a 5-bit shift register made of ***D*** FFs such that the complementary output ($\bar{Q}$) of the *rightmost* FF is connected to the D input of the *leftmost* FF. Assume that the initial state of this synchronous sequential circuit is one in which the leftmost FF is in set state while the remaining FFs are in reset states. Write the complete state table for this sequential circuit, starting with the given initial state. **Derive** the **minimum** decoding logic for the initial state (do not simply state it). Mention the length of a cycle, if any exists in the state transition diagram of the circuit. [8]

5 (a) Draw the complete gate diagram of a ***positive edge-triggered D***-type flip-flop (D FF) constructed using only NAND gates. Show that with D input either at 0 or 1, when the clock **changes** from 0 to1, the output Q will certainly follow the input D. **Also** show that now with the clock **remaining** at 1, **even if** D changes from 1 to 0 or from 0 to 1, the output Q will remain **unchanged**. Show how active **low asynchronous preset** and **clear** signals can be provided for this FF, which would cause the output Q to go to 1 and 0 respectively, regardless of all other inputs. [12]

(b) Plot the function $F(a,b,c,d) = \sum m(0,4,5,7,8,10,14,15)$ where a is the most significant variable on a Karnaugh map. From the K-map, find the two totally different minimal sum-of-products (SOP) expressions (i.e. the two SOP expressions have no common product term) for F. Note that the two SOP expressions will have the same cost, i.e. the number of terms and literals is the same in both. [6]

(c) In the context of design of an asynchronous circuit, define what is meant by a **critical race** condition. [2]

6 (a) How does a **Moore model** of a synchronous sequential circuit differ from a **Mealy model**? Consider a sequence detector that produces an output 1 each time the sequence 1010 or 1011 appears at the input. Overlapping is allowed. For example, a valid input-output pattern may be as follows:

input x : 0 0 1 1 0 1 0 1 1 0 1 1 0 1 1 0 1 0 1 0 0 ...
output z : 0 0 0 0 0 0 1 0 1 0 0 0 0 0 1 0 0 1 0 1 0 ...

Give the state diagram and the state table of such a sequence detector if **Mealy model** is followed to describe the behavior of the circuit. Next, derive the state transition table and diagram of the sequence detector corresponding to its **Moore model**. [8]

(b) A 2-input, 1-output synchronous sequential circuit is specified by the following state (and output) table. Reduce the number of states by applying the **Partitioning** technique. Clearly show how successive partitions are generated at consecutive steps. Finally, determine the **equivalence partition** and write the reduced state table for the given completely specified sequential circuit. [12]

Present State	Next state and output for different input conditions			
	$x_1x_2 = 00$	$x_1x_2 = 01$	$x_1x_2 = 11$	$x_1x_2 = 10$
A	D/0	D/0	F/0	A/0
B	C/1	D/0	E/1	F/0
C	C/1	D/0	E/1	A/0
D	D/0	B/0	A/0	F/0
E	C/1	F/0	E/1	A/0
F	D/0	D/0	A/0	F/0
G	G/0	G/0	A/0	A/0
H	B/1	D/0	E/1	A/0

Table 1: State table for a sequential circuit (Question 6 (b))

*** End of the Question Paper ***