INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

Date ..... FN / AN Time : ~~2~~ / 3 Hrs. Full Marks ....60..... No. of Students ..... 295 .....

Autumn / ~~Spring~~ Semester ..... Dept. ..... CSE, E&ECE, EE, IE ..... Sub. No. ..... EC 21103 .....

... 2nd .... Yr. B. Tech. (H) / ~~B. Arch (H)~~ / ~~M. Sc.~~ Sub. Name ..... INTRODUCTION TO ELECTRONICS .....

INSTRUCTIONS

1. **All waveform sketches / diagrams must be neatly drawn and clearly labeled.**
2. **The final answers (numerical values with unit) must be underlined or enclosed in a box.**
3. **For any value related to any device parameter or circuit parameter, which you may find not given with a problem, assume suitable value for such parameter.**
4. **Answers must be brief and to the point. Partial credit will be awarded for correct attempt.**
5. **Start working out the solution for every problem in a new page.**
6. **For each problem, please write the answers of all its parts together and avoid writing answers of its various parts at different locations in your answer-script.**

1. Problem on MOS Circuits: 20 points

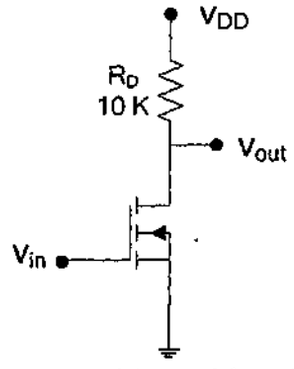

Figure 1. NMOS driver with resistor load

(1a) Refer to the circuit shown in Figure 1.
V_{Tn} = 1 V, $\mu_n C_{OX}$ = 100 uA/V^2, λ_n = 0 V^{-1}
W/L = 2 um / 1um, V_{DD} = 5 V, R_D = 10K ohm

Draw the output waveform for the following conditions:
(In each case show the max. and min. values of V_{out})

- $V_{in} = 2 + 0.1 \sin(2\pi \cdot 10^3 \cdot t)$ V [4]
- $V_{in} = 5 + 0.1 \sin(2\pi \cdot 10^3 \cdot t)$ V [4]

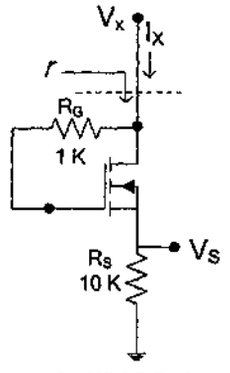

Figure 2. NMOS circuit

(1b) Refer to the circuit shown in Figure 2.
V_{Tn} = 1 V, $\mu_n C_{OX}$ = 100 uA/V^2, λ_n = 0 V^{-1},
W/L = 2 um / 1um, R_S = 10K ohm

When input voltage V_X varies from 0V to 5V, plot the following:

- Source voltage V_S vs. input V_X [4]
- Drain current I_X vs. input V_X [4]
- Small signal resistance, r (= $\Delta V_x / \Delta I_x$) vs. input V_X [4]

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2. Problem on OPAMP circuit: 10 points

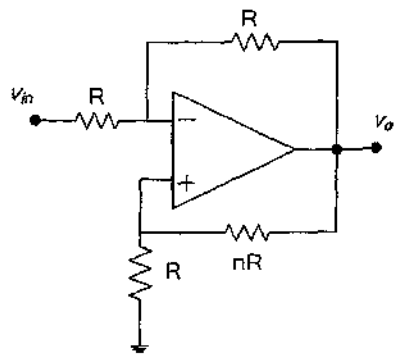

Figure 3. OPAMP circuit for (2a)

(2a) For the circuit in Figure 3, assume ideal OPAMP.

- For n > 1, find the voltage gain, v_o / v_{in}. [5]
- For n < 1, comment on how the circuit will behave. [1]

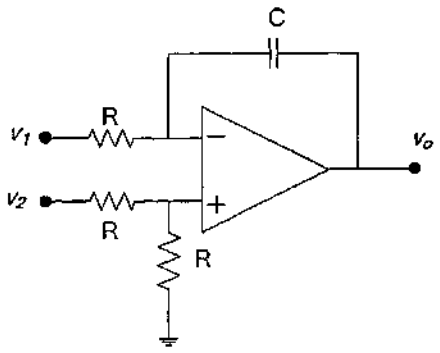

Figure 4. OPAMP Circuit for (2b)

(2b) For the circuit shown in Figure 4, assume ideal OPAMP.

- Express v_o in terms of v_1 and v_2. [4]

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3. Problem on OPAMP and Feedback circuits: 10 points

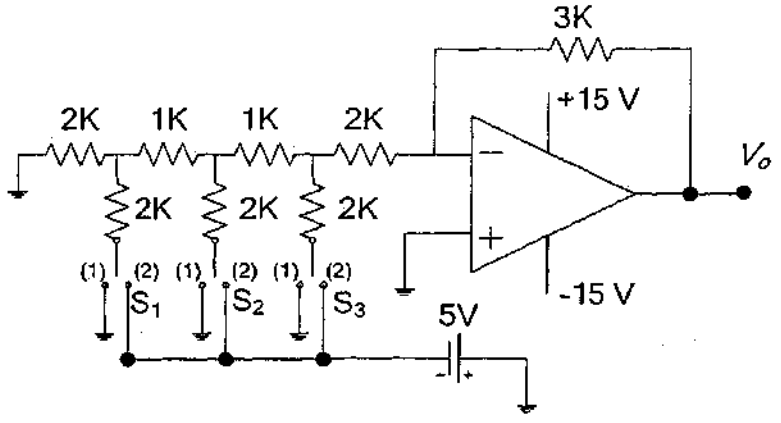

Figure 5. OPAMP Circuit for (3a)

(3a) Refer to the circuit shown in Figure 5. Each of the switches S_1, S_2 and S_3 can be either in position-1 (GND) or in position-2 (-5V).

- For all possible switch-position combinations, determine V_o. [5]

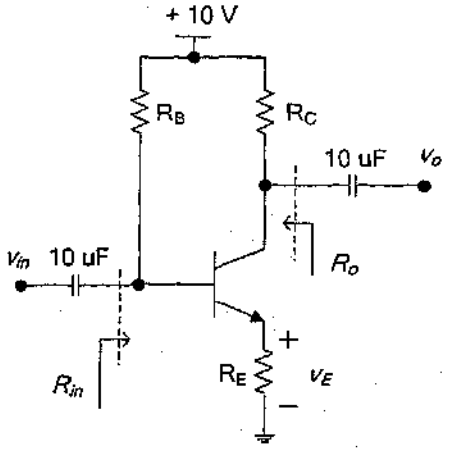

Figure 6. BJT Circuit for (3b)

(3b) Refer to the circuit shown in Figure 6. The output is taken as the voltage v_0 while the potential difference across R_E (= v_E) is used as the negative feedback signal. Ignore Early effect.

[1]

- Identify the nature of the feedback. [2]
- Find the expression for small-signal voltage gain, v_o/v_{in} [1]
- Find the expression for small-signal input impedance, R_{in} [1]
- Find the expression for small-signal output impedance, R_o

4. Problem on logic circuits: 10 points

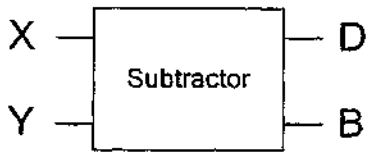

Figure 7. 1-bit Subtractor

(4a) Design the logic circuit using gates for the block shown in Figure 7, which subtracts the bit Y from bit X and outputs the difference bit D and a borrow bit B. [5]

(4b) Suitably cascade more than one blocks of Figure 7 to design a two bit subtractor which will subtract {Y1, Y0} from {X1, X0}. [5]

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5. Problem on logic circuits: 10 points

(5a) Simplify the logic circuit in Figure 8 using Karnaugh Map. [5]

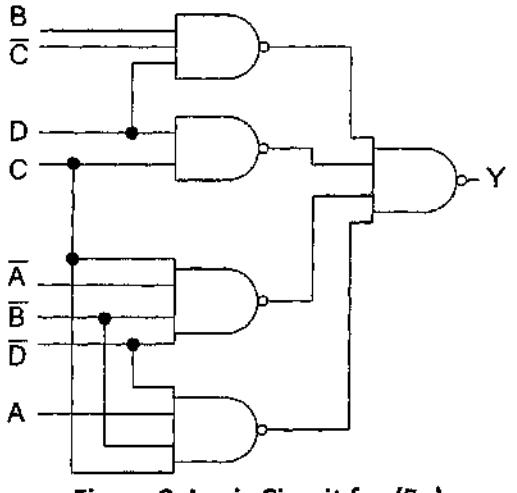

Figure 8. Logic Circuit for (5a)

(5b) For the circuit in Figure 9, sketch the Q output vs. time, with reference to the inputs A and B shown in Figure 10. Assume that the flip-flop is initially cleared. [5]

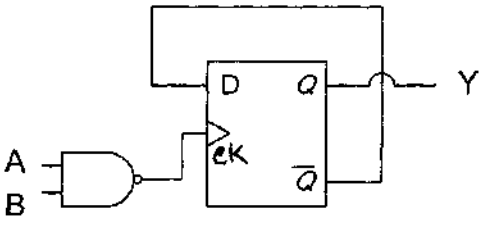

Figure 9. Logic Circuit for (5b)

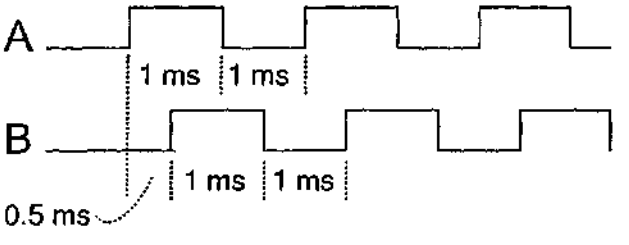

Figure 10. Input waveforms of A and B for (5b)