INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

Date: September, 2012 **Time**: 2 Hrs. Full Marks: 60 **Number of Students**: 240
Mid-Autumn Semester: 2012-2013 **Dept**: E&ECE **Subject Number**: EC 31003
B. Tech **Subject Name**: Digital Electronic Circuits

Instructions: This question paper consists of two pages. Answers to parts of a question must be written in one place. Otherwise, they will not be checked. Answer **all** the questions. Questions are self-explanatory and need no clarification.

1 (a) Algebraically minimize the following expressions algebraically (that is, **without** using Karnaugh maps). Mention the Boolean axioms and theorems applied at each step.

(i) $A\overline{B}C+B+B\overline{D}+AB\overline{D}+\overline{A}C$ [2]

(ii) $(\overline{A}+B+C+D)(B+F)(\overline{A}+C+D+\overline{F})$ [4]

(b) You are given a 3-input, 1-output circuit block such that with a, b, and c as inputs, the output obtained from the block is $F_1(a,b,c)=\overline{a}bc+a\overline{b}+\overline{b}\overline{c}$. Realize the unary NOT operation, binary AND, and binary OR operations using this block.
Hint: the block can be used more than once to realize an operation, and some of the inputs can be set to constants '0' or '1'. [6]

(c) (i) Prove that **NOR** operation is (or is **not**) associative. [2]
(ii) Show that the function $G(a,b,c,d)=a+bd+\overline{c}d$ can be implemented using only **2-input NAND** gates. [3]

(d) Find the values of the switching (two-valued) variables A, B, C, and D by solving the following set of simultaneous equations: $\overline{A}+AB=0$; $AB=AC$; $AB+A\overline{C}+CD=\overline{C}D$; [3]

2 (a) Realize a 4-variable function ***F(a, b, c, d)*** (***a*** being the most significant variable) by using only the smallest number of **4-to-1 multiplexers**. Draw the complete interconnection of the modules, clearly showing all the data inputs, the control (selection) inputs and the outputs of all the multiplexers. [6]

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(b) Assume that a 4-bit magnitude comparator module compares two **nibbles** or 4-bit binary numbers $A \equiv A_3A_2A_1A_0$ and $B \equiv B_3B_2B_1B_0$, and produces three outputs $(A=B)_{out}$, $(A>B)_{out}$, and $(A<B)_{out}$, depending on whether A is equal to B, A is greater than B, and A is less than B, respectively. Also, assume the presence of three inputs $(A=B)_{in}$, $(A>B)_{in}$, and $(A<B)_{in}$ to a comparator module conveying the results of comparing the higher-order nibbles of two multi-bit numbers from an identical comparator module. You are required to use two such modules in order to compare two 8-bit numbers $\mathbf{X \equiv X_7 \ldots X_0}$ and $\mathbf{Y \equiv Y_7 \ldots Y_0}$. Show all the required interconnections and write the complete logic expressions for the three output functions of a 4-bit module. [6]

(c) Explain how a 4-bit **carry look-ahead adder (CLA)** works faster than a 4-bit ripple carry adder. Define carry propagate function P_i and carry generate function G_i for each stage i of a 4-bit CLA. Let $A \equiv A_3A_2A_1A_0$, $B \equiv B_3B_2B_1B_0$ and C_{-1}(carry input) be the inputs of a 4-bit CLA. Write the expressions for all the four carry output functions of a 4-bit CLA completely in terms of the inputs. Show clearly how the 4-bit sum $S \equiv S_3S_2S_1S_0$ and the carry output C_4 are produced in such a CLA. [8]

3. (a) Write the truth table and draw the Karnaugh map of a 4-variable **majority** function ***M(a, b, c, d)*** (***a*** being the most significant variable) which is equal to 1 when the majority of its arguments assume the value 1. From the Karnaugh map, obtain the minimized **P-O-S (product-of-sums)** expression for ***M(a, b, c, d)***. Implement ***this*** minimized P-O-S expression using **only** the smallest number of **2-input NAND** gates. Assume that all variables as well as their complements (i.e. $a, \bar{a}, \ldots, d, \bar{d}$) are provided as inputs. Draw the gate diagram. How many 2-input NAND gates are required? [10]

(b) What are the advantages of designing multiple-output combinational logic circuits by **PLA** (programmable logic array) rather than discrete logic gates?
Implement a 2-bit ripple carry adder (meant for adding two 2-bit binary numbers $\mathbf{A_1A_0}$ and $\mathbf{B_1B_0}$ say) and a carry input $\mathbf{C_{-1}}$ by a PLA which has four dedicated input pins, three dedicated output pins and two bidirectional (input/output) pins. Write all the relevant logic equations. Draw the complete layout for the PLA, clearly showing the locations of the fuses and how different product terms and outputs are realized. [10]

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