INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

Date: September, 2010 Time: 2 Hrs. Full Marks: 60 Number of Students: 130

Mid-Autumn Semester 2009-2010 Deptt. E&ECE Subject Number: EC 31003

B. Tech Subject Name: Digital Electronic Circuits

Instructions: This question paper consists of two pages. Answers to parts of a question must be written in one place. Otherwise, they will not be checked. Answer **all** the questions.

1 (a) Simplify the following expressions using laws of Boolean algebra (do **not** use Karnaugh maps).

(i) $A + B\,[AC + (B + \overline{C})D]$ [3]

(ii) $A\overline{B}C + B + B\overline{D} + AB\overline{D} + \overline{A}C$ [3]

(b) You are given a 3-input, 1-output circuit block such that with a, b, and c as inputs, the output obtained from the block is $F_1(a,b,c) = \bar{a}bc + a\bar{b} + \bar{b}\bar{c}$. Realize the unary NOT operation, binary AND, and binary OR operations using this block.
Hint: the block can be used more than once to realize an operation, and some of the inputs can be set to constants '0' or '1'. [6]

(c) Find the values of the switching (two-valued) variables A, B, C, and D by solving the following set of simultaneous equations: $\overline{A} + AB = 0$; $AB = AC$;
$AB + A\overline{C} + CD = \overline{C}D$; [4]

2 (a) Use Karnaugh map to minimize the expression

$F_2(a,b,c,d) = \prod M(2,8,9,10,11,12,14)$ (where a is the most significant variable) into a product-of-sums (POS) form. Implement this POS form of the function using only **NAND** gates. [8]

PTO

(b) Use a 3-to-8 decoder with active low outputs and combinational gate(s) to realize the function $F_3(a,b,c)=\sum m(2,3,7)$ where a is the most significant variable. Draw the complete circuit connections. [3]

(c) Use an 8-to-1 multiplexer to implement the function

$F_4(a,b,c,d)=\sum m(0,1,2,3,4,10,11,14,15)$ where a is the most significant variable. Write the complete truth table. Use the variables a, b, and c as the selection control inputs of the multiplexer. Show the complete circuit connections. [9]

3. (a) Assume that a 4-bit magnitude comparator module compares two 4-bit numbers $A \equiv A_3A_2A_1A_0$ and $B \equiv B_3B_2B_1B_0$, and produces three outputs $(A=B)_{out}$, $(A>B)_{out}$, and $(A<B)_{out}$, depending on whether A is equal to B, A is greater than B, and A is less than B, respectively. You are required to use two such modules in order to compare two 8-bit numbers $X \equiv X_7 \ldots X_0$ and $Y \equiv Y_7 \ldots Y_0$. Show all the required interconnections and write the complete expressions for the three output functions of a 4-bit module. [6]

(b) Explain how a 4-bit carry look-ahead adder (CLA) works faster than a 4-bit ripple carry adder. Define carry propagate function P_i and carry generate function G_i for each stage i of a 4-bit CLA. Let $A \equiv A_3A_2A_1A_0$, $B \equiv B_3B_2B_1B_0$ and C_{-1}(carry input) be the inputs of a 4-bit CLA. Write the expressions for all the four carry output functions of a 4-bit CLA completely in terms of the inputs. [2+6=8]

(c) How does a programmable read-only memory (PROM) device differ from a programmable logic array (PLA) device? Realize the following three 3-variable functions using a PROM: $Y_0 = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + A\overline{B}\,\overline{C} + A\overline{B}C$;
$Y_1 = \overline{A}\,BC + \overline{A}\,B\overline{C} + ABC + AB\overline{C}$; and $Y_2 = \overline{A}\,\overline{B}\,C + \overline{A}\,BC + A\overline{B}\,C + ABC$; Draw the complete circuit layout using proper symbols. Comment on advantage/disadvantage of realizing the three above functions by a PLA rather than a PROM. [1+6+3=10]