RR

Basic Electronics (EC21101)

Mid-Autumn Semester Examination 2012-13.

Department of E & ECE, Indian Institute of Technology, Kharagpur.

Answer all the questions. All symbols have their usual meaning.

Time – 2 hours. Total marks = 50.

Marks distribution – (1×10) + (1×10) + (3×10).

1(a) n-type silicon is obtained by

(*i*) Doping with pentavalent element. (*ii*) Doping with tetravalent element.
(*iii*) Doping with trivalent element. (*iv*) Doping with a mixture of trivalent and tetravalent element.

(b) The breakdown mechanism in a lightly doped *p-n* junction under reverse bias condition is called

(*i*) Avalanche breakdown. (*ii*) Zener breakdown.
(*iii*) Breakdown by tunnelling. (*iv*) High voltage breakdown.

(c) In a full-wave rectifier without filter, the ripple factor is

(*i*) 0.482 (*ii*) 1.21
(*iii*) 1.79 (*iv*) 2.05

(d) Schottky barrier diode is a junction of

(*i*) Heavily doped *p*- and heavily doped *n*-type materials.
(*ii*) Metal and heavily doped *p*-type material,
(*iii*) Metal and moderately doped *n*-type material.
(*iv*) Heavily doped *p*-type and intrinsic semiconductor.

(e) The important characteristic of an emitter-follower is

(*i*) High input impedance and high output impedance.
(*ii*) High input impedance and low output impedance.
(*iii*) Low input impedance and low output impedance.
(*iv*) Low input impedance and high output impedance.

(f) In a CE – connected transistor amplifier with voltage gain A_v, the capacitance C_{bc} is amplified by a factor

(*i*) A_v. (*ii*) A_v+1.
(*iii*) A_v^2. (*iv*) $\sqrt{(A_v+1)}$.

(g) Two stages of a BJT amplifier are cascaded by RC coupling. The voltage gain of the first stage is 10 and that of the second stage is also 10. The overall gain of the coupled amplifier is

(*i*) 10×10. (*ii*) 10+10.
(*iii*) $(10+10)^2$. (*iv*) (10×10)/2.

(h) When a step-input is given to an op-amp integrator, the output will be

(*i*) A ramp. (*ii*) A sinusoidal wave.
(*iii*) A rectangular wave. (*iv*) A triangular wave with dc bias.

(i) For an op-amp having differential gain A_d and common-mode gain A_c the CMRR is given by

(*i*) $A_d + A_c$ (*ii*) A_d/A_c
(*iii*) A_c/A_d (*iv*) $A_d - A_c$

(j) For a voltage follower using an ideal op-amp, the input and output resistances are, respectively,

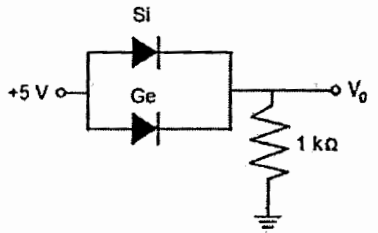
(*i*) Infinite and zero. (*ii*) Zero and infinite.
(*iii*) Zero and zero. (*iv*) Infinite and infinite.

2(a) A sample of *Si* is doped with donor density $N_d = 10^{16}$ /c.c. If $n_i = 1.5 \times 10^{10}$/c.c., calculate the hole density p_0 at the room temperature.

(b) A series R-C circuit consist of a resistor of 100 Ω and a capacitor of 4.7μF. Calculate the time constant τ of the circuit.

(c) A *Si pn*-junction has a reverse saturation current I_S = 10 nA at the room temperature. Calculate the junction current when the applied voltage is 0.7 V forward bias.

(d) In the following figure, what is the value of V_0?



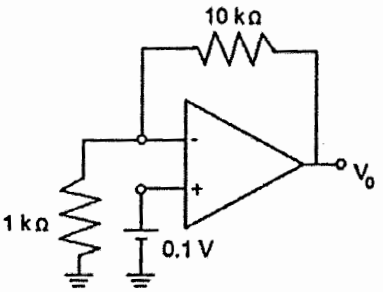
(e) Calculate the magnitude of the dc component at the output of a half wave rectifier made of an ideal diode for an input voltage $v_i = 17\sin 314.1t$.

(f) The power dissipation factor of the transistor 2N3904 is P_D = 600 mW at room temperature. For a bias voltage V_{cc} = 12 volt, calculate the maximum allowed collector current I_c.

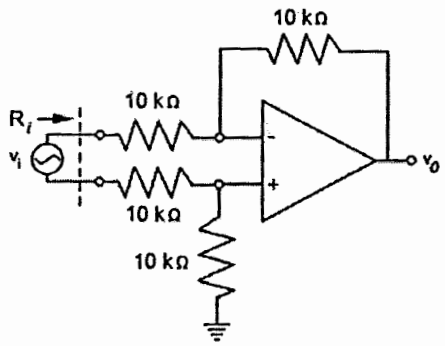
(g) Calculate the stability factor for the base-bias configuration made of an *npn* transistor. h_{FE} = 130, R_c = 1 kΩ and R_B = 220 kΩ.

(h) The small signal hybrid parameters of a transistor are r_π =1 kΩ, g_m = 100 mA/V and $r_0 = \infty$. Then calculate the CE-circuit forward current gain of the transistor.

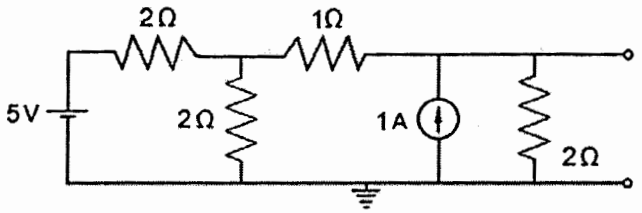
(i) Calculate V_0 in the following circuit.



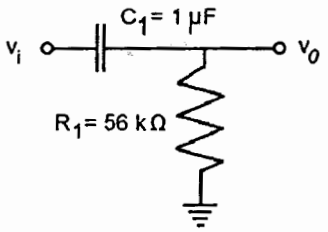
(j) What is the value of differential input resistance R_i in the following circuit?



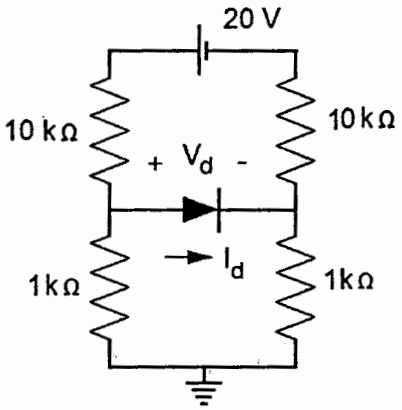
3.(a) Draw the equivalent Thevenin's source for the following circuit.



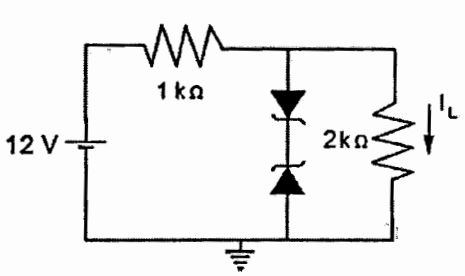
(b) The following circuit has a ±10 V, 1 kHz square wave as input. Calculate the tilt on the output waveform.

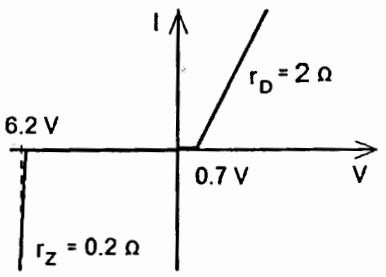


(c) A *Si*-diode is used in the following circuit. Determine the diode voltage V_d and the current I_d.

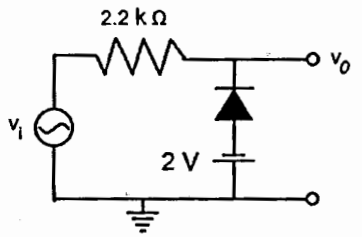


(d) Calculate the current flowing through the load I_L. The diode characteristic is shown on the right side.

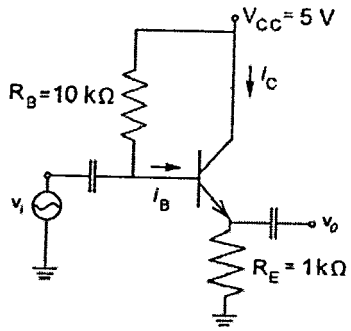




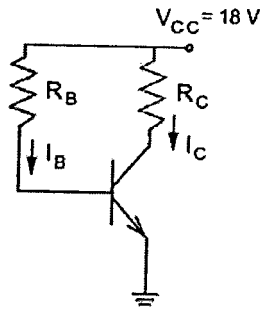
(e) Draw the output wave form for the following circuit if the diodes are ideal and the input voltage is $v_i = 8.5 \sin 314.1t$.



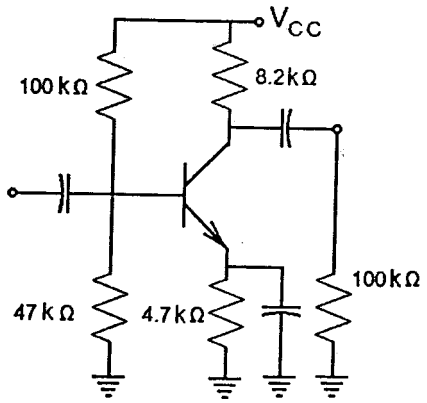
(f) In the following emitter follower circuit, the transistor has a β of 100. Calculate the bias currents and voltages.



(g) Check whether the following *Si*-transistor is operating in active or saturation region. $R_B = 470\ k\Omega$, $R_C = 10\ k\Omega$, and $h_{FE} = 100$.



(h) Calculate the input impedance Z_i, output impedance Z_0 and mid-band voltage gain A_v of the CE amplifier. All the capacitors have high values ($h_{ie} = 2.1\ k\Omega$, $h_{fe} = 70$, $h_{0e} = 10^{-6}\ \Omega$).



(i) Design an inverting amplifier having a gain of -10 and an input resistance of 100 kΩ.

(j) In the following circuit, a square wave of height 1 V and frequency 500 Hz is set as v_i. Draw the output wave form. R = 10 kΩ and C = 10 nF and the op-amp is specified to saturate at ±15 V.