INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

November 2009 Time: 3 hours Full Marks: 50 No. of Students: 200
Autumn Semester 2009-2010 E&ECE Department Sub. No. EC21101
Second Year B.Tech. Sub. Name: Basic Electronics

Instructions:
All Questions are to be answered. Full Marks for each question are shown in brackets. All symbols have their usual meaning. Questions in parts i.e (a) , (b) should be answered in sequence.

1. For W/L = 50/0.5 and I_D (saturation current) = 0.5 mA, calculate the transconductance and output impedance of both NMOS and PMOS devices. Also find the "intrinsic gain" of the transistor defined as $g_m r_o$, where g_m and r_o are the transconductance and output impedance of MOS transistor.
   For NMOS: $t_{ox} = 9x10^{-9}$ m, $\mu_n = 350$ cm^2/Volt-Sec, $\lambda = 0.1$ / V
   For PMOS: $t_{ox} = 9x10^{-9}$ m, $\mu_p = 100$ cm^2/Volt-Sec, $\lambda = 0.2$ / V (5 marks)

2. If g_m and r_o are the transconductance and output impedance of an NMOS transistor, derive the expression for the intrinsic gain (A_0) of the transistor in terms of I_D and W/L. Plot the intrinsic gain (A_0) as a function of I_D with L as a parameter. Note that I_D is the saturation current, W is the width of the transistor, L is the length of the transistor and λ (channel length modulation) which is proportional to 1/L. (5 marks)

3. An amplifier provides 8 V output under unloaded condition. When a load of 8 Ω is connected at its output, the voltage drops down to 1 V. Find out the input resistance of the unity voltage gain buffer that is to be put between the amplifier and the load so that the output voltage across the same load would be 6 V. Given that the output resistance of the buffer is 2 Ω. (5 marks)

4. An amplifier without feedback is having a voltage gain of 100 and a current gain of 80 and an input resistance of 600 Ω. Find out the input resistance offered when voltage series feedback is employed with a feedback factor of 0.025. What would be the input resistance if current shunt feedback is employed with the same feedback factor? (5 marks)

5. An ADC with SNR of 74 dB has an input signal of 5sin(2πft) Volts, find rms quantization noise and the resolution in mV. If the conversion time for this ADC is 8 μs, sample & hold aperture time is 0.1 μs and acquisition time is 2 μs find the maximum input signal frequency to avoid aliasing? (5 marks)

6. In the R-2R network shown in Fig.1, find V_O using Thevnin's equivalent circuit when B_2 and B_3 are connected to ground and B_1 is connected to 10V. What is the error in V_O to reach full scale value of 10V when B_1, B_2 and B_3 all are at 10V? To reduce this error to less than 0.1 V how many B inputs are required in an enhanced R-2R network? (5 marks)

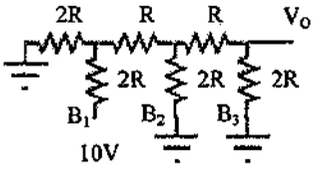

Fig. 1

7. P and Q are each 2 bit binary numbers. Write the Truth table and canonical sum of the logic function for P = Q output. Find the minimum number of 2 input NAND gates needed to realize this logic function. For this logic function if a ROM is used with control inputs to select any of the four conditions, P > Q, P = Q, P < Q and don't compare (that is, disable output) to give one line output, find memory size of the ROM? (5 marks)

Please turn over

8. a) Refer to the circuit in Fig. 2. Assuming the op-amp is an ideal one, calculate the value of V_{out} for $V_1 = 0.5V$, $V_2 = 0.2V$, $R_i = 3k\Omega$ and $R_f = 33k\Omega$. If the op-amp gain is changed to 50 (while its input and output resistances remain very high and very low respectively) then what is the value of V_{out} for $V_1 = 0.5V$, $V_2 = 0V$, $R_i = 2.5k\Omega$ and $R_f = 25\ k\Omega$. (5 marks)

b) Refer to the circuit in Fig. 3. Assume the op-amp and the diode are ideal. Neatly sketch voltages V_x and V_y along with the input signal V_{in} for the following two cases:

Case 1: $V_{in} = 2\ Sin\ (2000\pi t)$ Volts

Case 2: $V_{in} = \sqrt{2} + 2\ Sin\ (2000\pi t + \pi)$ Volts (5 marks)

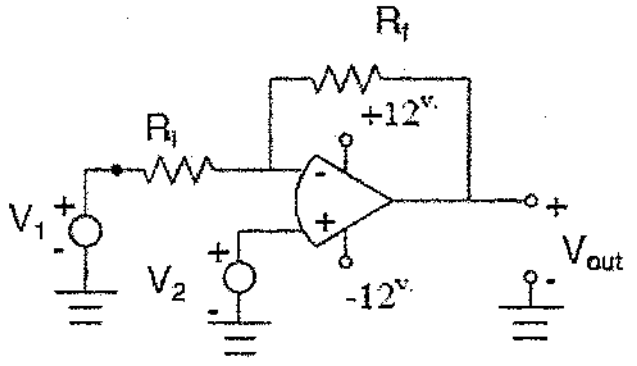

Fig. 2

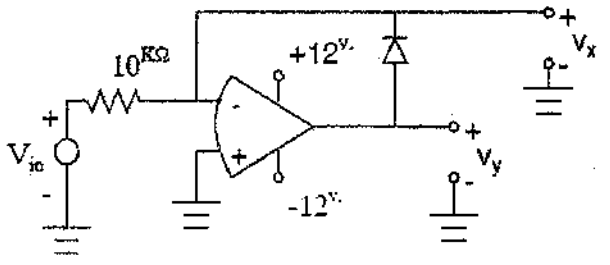

Fig. 3

c) Refer to the two circuits and the sketch of their input signal in Fig. 4. Neatly sketch the voltages V_x and V_y. Assume that the op-amp is an ideal one and R.C = 20µsec. (5 marks)

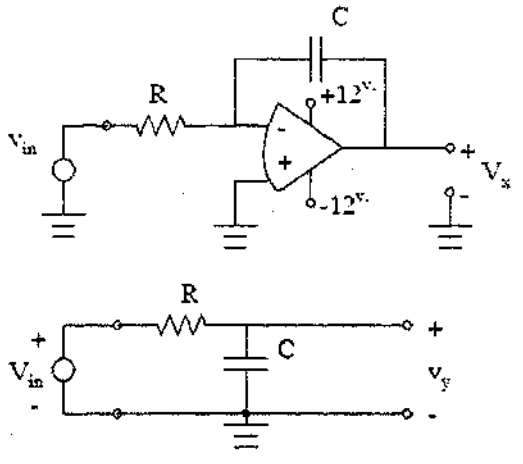

Fig. 4

Sketch of V_{in}