INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

Date.....FN/AN Time: 3 Hrs Full Marks: 100 No. of Students: 177
Autumn Semester Deptt.: E & ECE Sub. No. : EC21101
2nd year B.Tech (H)/ M.Sc. Sub. Name: Basic Electronics

Note: Attempt all the questions.
Answer to all the parts of a question should be attempted in the sequence and at one place only.

Q.1 (a) What is the value of the current and junction potential in a short circuited p-n junction diode and why? 2

(b) What is Pauli's exclusion principle. 2

(c) What is the difference between electron hole recombination in a semiconductor bar and collision between an electron and positron in free space? 2

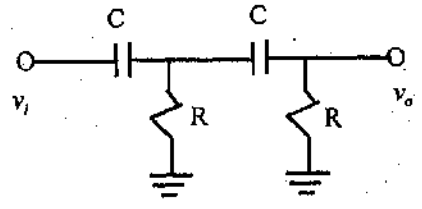
(d) What happens to holes at an Ohmic contact between semiconductor bar and external circuit? 2

(e) Why the mobility of an electron is typically higher than that of a hole in a particular intrinsic semiconductor at a particular temperature? 2

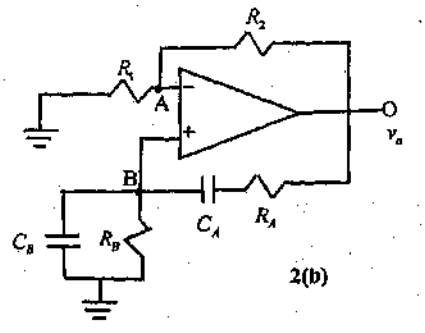
(f) In a simple circuit between two points A and B lies a diode and a resistance of value R Ohm. Voltage v(t) volts is applied between A and B and it has got value of +V volts in time interval [0 sec, s sec] and -1.2V volts for all time t > s sec. The current through the circuit is i(t) ampere and voltage drop across the diode is u(t) volts. Plot (i) i(t) vs. t (ii) u(t) vs. t., and (iii) Explain the physics behind these curves. 2+2+3+3

Q.2 (a) Derive the transfer function for the network given in Fig. 2(a). Can this network be used to realize 180° phase shift? 8

(b) An oscillator circuit is drawn in Fig. 2(b). (i) Identify the frequency selective feedback network and determine its transfer function $\beta(s)$. (ii) Derive the expression for the frequency of oscillation. 4+8



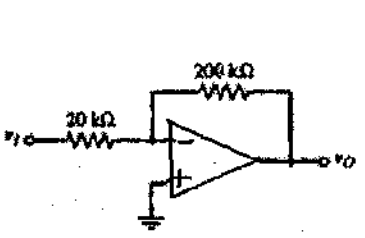
2(a)



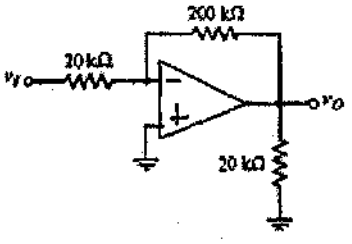
2(b)

Q. 3 Design a single pole low-pass filter with a gain of 10 in the pass band and 3 dB frequency of 5 kHz. 10

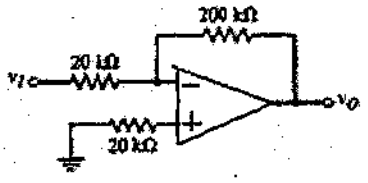
Q. 4 Assuming all the op-amps are ideal, determine the voltage gain and the input resistance of the amplifier configurations given below. 5X4



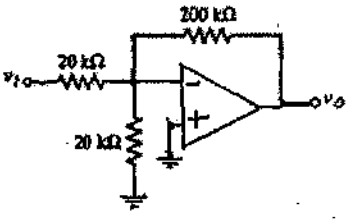
(a)



(b)



(c)



(d)

Q.5 (a) Draw the combinational logic circuit for the following expressions with AND-OR gates: 4+4

$Y = A\bar{B}C + AB + \bar{A}BC + C$

Y = F(A, B, C, D) = ∑m(1,2,3,6,8,9,10,12)

(b) Draw the Karnaugh map for the equation

Y = F(A,B,C,D) = ∑m(0,1,2,4,5,6,8,9,10,12,13).

Simplify it with the help of the map and draw the simplified logic circuit. 2+4

Q.6 (a) Draw a 6-input 1-output *multiplexer* with the help of AND,OR and NOT gates. Show the date lines and the related control lines so that only one data line is connected to the output at a time. 4

(b) Develop an edge-triggered J-K flip-flop from a basic R-S flip-flop and show the truth tables. (Hint of various stages: R-S flip flop --- clocked R-S flip flop --- Edge-triggered R-S flip flop --- edge-triggered J-K flip flop). 6

(c) Draw a SERIAL IN – SERIAL OUT 6-bit shift register with the help of 6 D- flip flops. Show the timing diagram for the 6 flip flop outputs Q, R, S, T, U, V when the serial bits 1011 is given at the D input of first flip flop. 6