INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

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B. Tech Subject Name: Digital Electronic Circuits

Instructions: This question paper consists of **four** pages. Answers to parts of one question must be written in one place. Otherwise, they will **not** be checked. Answer **any five** questions. Note carefully that **only** the **first five** answers will be checked even if you answer all six questions.

1 (a) Plot the function $F(a,b,c,d)=\sum m(0,4,5,7,8,10,14,15)$ where a is the most significant variable on a Karnaugh map. From the K-map, find the two totally different minimal sum-of-products (SOP) expressions (i.e. the two SOP expressions have no common product term) for F. Note that the two SOP expressions will have the same cost, i.e. the number of terms and literals is the same in both. [6]

(b) Realize the following three switching functions by means of a 3-input 3-output PROM (programmable read-only memory), namely $P(a,b,c)= ab + \overline{b}\,c$; $Q(a,b,c)= (a+\overline{b}+c)(\overline{a}+b)$; and $R(a,b,c)= a + bc$. Note that a is the most significant variable. Draw the complete AND and OR arrays, showing clearly where the fuses (links) will remain after programming. [9]

(c) Realize the function $G(a,b,c)= ab + \overline{a}\,\overline{b}$ (where a is the most significant variable) by a 3-to-8 decoder with active low outputs and only 2-input NAND gates. Assume that the decoder has two active low and one active high enable inputs. Draw the complete logic diagram. [5]

2 (a) A memory module contains 16384 bits. How many address lines will be required if the memory is (i) byte-organized and (ii) bit-organized? [2]

(b) Draw a neat diagram to show how the memory cells are arranged in a two-dimensional bit-organized 16×1 memory. Take any one cell and show how it is addressed. [5]

(c) Draw the complete transistor diagram of a bipolar static RAM cell including the read amplifier, the write amplifier and the control logic circuit. Referring to your diagram, briefly explain how one can read from and write into the memory cell. [13]

3 (a) The state diagram of a synchronous sequential circuit with one input and one output is shown in Figure 1. For the state assignment A = 001; B = 010; C = 011; D = 100; and E = 101, implement the circuit using positive edge-triggered *SR* flip-flops. Give the excitation requirement of an *SR* flip-flop as a table. Write the state transition table, the excitation table and the output table for the given circuit. Minimize the size of the required combinational logic. Draw the circuit diagram. [14]

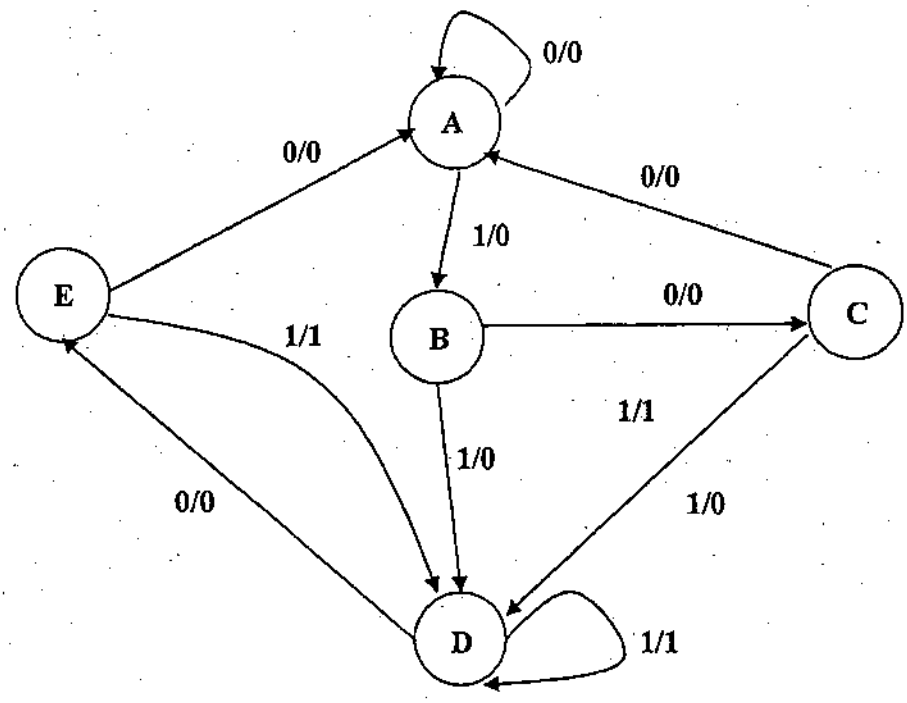

Figure 1 State diagram of a sequential circuit (Question 3(a))

(b) When a certain binary serial communication channel operates correctly, all blocks of 0s are of *even* length and all blocks of 1s are of *odd* length. A synchronous sequential (finite state) machine will produce an output *z=1* whenever a discrepancy from the above pattern is detected. A valid input-output pattern may be as follows :

input x : 0 0 1 0 0 0 1 1 1 0 1 1 0 0 ...
output z : 0 0 0 0 0 0 1 0 0 0 1 0 1 0 ...

Draw the state transition diagram and write the state table for the pattern detector. Describe each state in terms of the associated input sequence. Do **not design** the corresponding circuit. [6]

4 (a) Draw the basic structure of a shift register (made of a chain of D flip-flops or D FFs) which can be adapted to function as a sequence generator. How many FFs are required to generate a sequence of length N? Generate the sequence $S = \cdots 1011110 \cdots$ using such a shift register consisting of the minimum possible number of D FFs. The same sequence should appear repeatedly at the output of each D FF (though not at the same time). You must show the complete state table for the synchronous sequential circuit. Design the circuit for which the combinational component, if any, should be of minimum complexity. Draw the complete logic diagram of the circuit. [12]

(b) Draw the circuit diagram for a 5-bit shift register made of D FFs such that the complementary output ($\bar{Q}$) of the rightmost FF is connected to the D input of the leftmost FF. Assume that the initial state of the synchronous sequential circuit is one in which the leftmost FF is in set state while the remaining FFs are in reset states. Write the complete state table for the circuit, starting with the given initial state. **Derive** the **minimum** decoding logic for the initial state (do not simply state it). Mention the length of a cycle, if any exists in the state transition diagram of the circuit. [8]

5 (a) Draw the complete gate diagram of a ***positive edge-triggered*** D-type flip-flop (D FF) constructed using only NAND gates. Show that with D input either at 0 or 1, when the clock **changes** from 0 to1, the output Q will certainly follow the input D. **Also** show that now with the clock **remaining** at 1, **even if** D changes from 1 to 0 or from 0 to 1, the output Q will remain **unchanged**. Provide active low asynchronous preset and clear signals for the FF which would cause the output Q to go to 1 and 0 respectively, regardless of all other inputs. [12]

(b) Show how an SR flip-flop (FF) can be converted to a JK FF. That is, you have actually an SR FF which will be made to behave like a JK FF with the addition of two external inputs J and K and a combinational circuit whose outputs are fed as excitation inputs to the available SR FF. Write the complete conversion table and design the combinational circuit with minimum size. Draw the logic diagram of the complete circuit. [8]

6 (a) Show how a serial adder can be designed as a (**Mealy model**) synchronous sequential circuit with two input terminals (at which the successive bits of the addend input and the augend input are applied) and a single output corresponding to the sum. Draw the state transition diagram of the serial adder. From this, draw the Algorithmic State Machine (ASM) chart (diagram) of the serial adder. [8]

(b) A 2-input, 1-output synchronous sequential circuit is specified by the following state (and output) table. Reduce the number of states by applying **Implication Table** method. Clearly show the consecutive steps. Finally, write the reduced state table for the given completely specified sequential circuit. [12]

Present State	Next state and output for different input conditions			
	$x_1x_2 = 00$	$x_1x_2 = 01$	$x_1x_2 = 11$	$x_1x_2 = 10$
A	D/0	D/0	F/0	A/0
B	C/1	D/0	E/1	F/0
C	C/1	D/0	E/1	A/0
D	D/0	B/0	A/0	F/0
E	C/1	F/0	E/1	A/0
F	D/0	D/0	A/0	F/0
G	G/0	G/0	A/0	A/0
H	B/1	D/0	E/1	A/0

Table 1: State table for a sequential circuit (Question 6 (b))

*** End of the Question Paper ***