INDIAN INSTITUTE OF TECHNOLOGY

Date: 18th **Nov 2011**, FN/AN, Time: **3 Hrs.**, Full Marks: **60**, Dept. : **CS/EE/EE/IE**, No. of Students : **352**

2nd Yr. B.Tech (H), **End Autumn** Semester, Sub. No.: **EC21103**, Sub. Name: **Introduction to Electronics**

Instruction: ___ Answer **all** questions.

- All waveform sketches / diagrams must be neatly drawn and clearly labeled. Answers must be brief and to the point.
- The final answers (numerical values with unit) should be underlined or enclosed within box.
- For every Question No., start your answer from a new page.
  Avoid writing answers of the various parts of a single question at different locations in your answer-script.
- For any value related to any device parameter or circuit parameter, which you may find not given with a problem, assume suitable value for such parameter.

Q 1. Problems on OPAMP Circuits and Feedback: 20 Marks

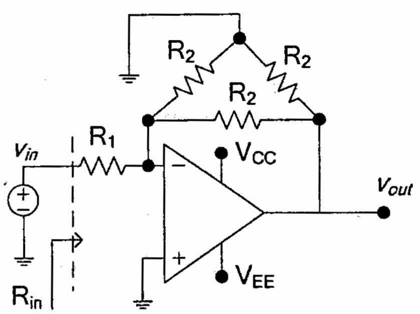

Figure 1. OPAMP Circuit (Q 1.A)

Q 1.A) Given, OPAMP open loop / forward gain (A_{OL})=∞, OPAMP input resistance($R_{i,op}$)=∞, OPAMP output resistance ($R_{o,op}$) = 0 Ω, R_2 = 1 kΩ, R_1 = 500 Ω, V_{CC} = 5 V, V_{EE} = -5V, Saturation voltages are +4 V and -4 V.

$V_{in} = A + B \sin(2\pi \cdot 1\text{ kHz} \cdot t)$

Q 1.A.1) Find the value of closed loop voltage gain, V_{out}/V_{in}. [2]
Q 1.A.2) Find the value of input impedance (R_{in}) [1]
Q 1.A.3) Plot V_{out} and V_{in} if A = 1 V, B = 1 V [1.5]
Q 1.A.4) Plot V_{out} and V_{in} if A = 1 V, B = 3 V [1.5]

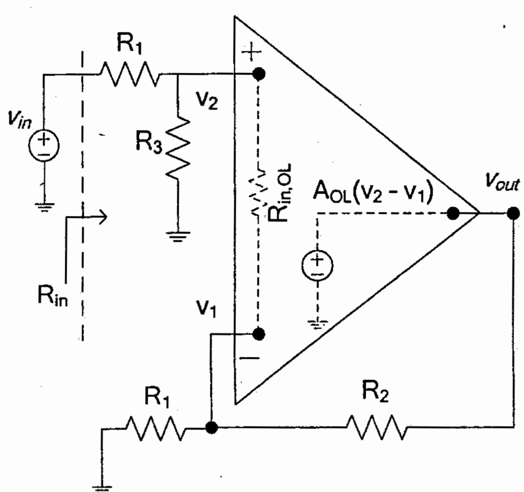

Figure 2. OPAMP Circuit (Q 1. B)

Q 1. B) OPAMP input resistance($R_{in,oL}$) = ∞, $R_2 = 2R_1$ = 1 kΩ.

Q 1. B.1) Find V_{out}/V_{in} expression and value, for OPAMP open loop gain (A_{OL}) = ∞, $R_3 = \infty$ [1.5]
Q 1. B.2) Find input impedance (R_{in}) for $A_{OL}=\infty$, $R_3 = \infty$ [1]
Q 1. B.3) Find V_{out}/V_{in} expression and value, for $A_{OL}=\infty$, and R_3 = 1 kΩ [1.5]
Q 1. B.4) Find input impedance (R_{in}) for $A_{OL}=\infty$, and R_3=1 kΩ [1]
Q 1. B.5) For A_{OL} = 1000, R_3 = 1 kΩ, find the expression and value of V_{out}/V_{in}. [2.5 +.5]
Q 1. B.6) Identify the type of feedback: What kind of output sampling and what kind of input mixing? [2]
Q 1. B.7) Find the expression and value of feedback factor (β)? [2]
Q 1. B.8) For A_{OL} = 1000, R_3 = 1 kΩ, derive V_{out}/V_{in} using the concept of feedback . [2]

Q 2. Problems on Transistor Amplifier and Feedback: 20 Marks

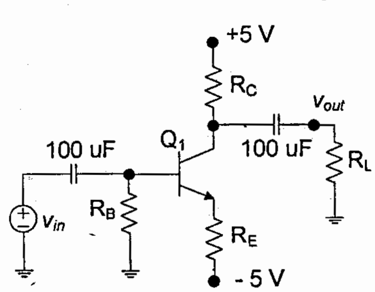

Figure 3. BJT Circuit (Q 2.A)

Q 2.A) Consider the amplifier circuit using npn BJT as shown in Figure 3.
β = 100, $V_A = \infty$, $V_{BE,ON}$ = 0.7 V, Thermal voltage, V_{TH} = 26 mV
Circuit parameters: $R_C = R_L$ = 4.9 KΩ, R_B = 419.9 KΩ, R_E = 100 Ω

Q 2.A.1) Find the values of I_B, V_B, I_C, and V_C. [2]
Q 2.A.2) Draw the small signal model of the circuit in Figure 3. [2]
Q 2.A.3) Obtain the expression for A_V and the value. [2]
Q 2.A.4) Identify the type of feedback i.e. what kind of output sampling and what kind of input mixing. [2]
Q 2.A.5) Explain why the feedback is a negative feedback? [1]

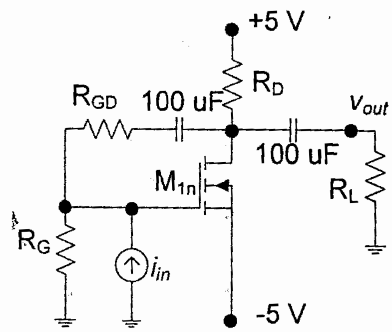

Figure 4. MOSFET Circuit (Q 2.B)

Q 2.B) NMOSFET M_{1n} parameters: V_{Tn} = 1 V, $\mu_n C_{OX}$ = 100 μA / V^2, λ = 0 V^{-1}, (W/L) = 2 μm / 1.6 μm; R_D = 5 KΩ, R_L = 5 KΩ, R_G = 100 kΩ, R_{GD} = 125 kΩ

The AC input current, i_{in} = 100 . sin(2π . 100 Hz . t) mV

Q 2.B.1) Find the values of I_D and V_D. [1]

Q 2.B.2) Identify the feedback topology i.e. what kind of sampling at output and what kind of mixing at input. [2]

Q 2.B.3) Draw the small-signal circuit in Figure 4 without feedback. Obtain the expression and value of the open-loop gain, $A_{OL}=v_{out}/i_{in}$ [in V/A]. [1+2 +1]

Q 2.B.4) Now in the above small signal model put R_{GD} i.e. feedback and find the closed loop gain $A_{CL}= v_{out}/i_{in}$ [in V/A]. [2]

Q 2.B.5) From the above closed loop gain A_{CL} identify the expression and value of feedback factor (β). [2]

Q 3. Problems on Digital Electronics: 20 Marks

Q 3.A.1) Find the decimal equivalent of the binary number $(01011011)_2$. [1]
Q 3.A.2) Find the 8-bit binary equivalent (2's complement form) of the decimal number $(-125)_{10}$. [1]
Q 3.A.3) What is the 8-bit result of $(00100001)_2 + (00011001)_2$? (Both the numbers are in 2's complement form) [1]
Q 3.A.4) What is the 8-bit result of $(00010111)_2 - (01010101)_2$? (Both the numbers are in 2's complement form) [1]

Q 3.B) Assuming both the normal input (e.g. A) and the complement input (e.g. A')are available, implement the following logic functions:
Q 3.B.1) F_1 = **A + B' D' + C D'** using only NAND gates. You may use NAND gates more than 2 inputs, if required. [2]
Q 3.B.2) F_2 = **A' B' + C' D' + B' C'** using only NOR gates. You may use NOR gates more than 2 inputs, if required. [2]

AB → / CD ↓	00	01	11	10
00	1			1
01				
11				
10	1			X

Figure 5. Karnaugh Map (Q 3.C.1)

Q 3.C.1) What is the logic function in the simplest form for the Karnaugh Map shown in Figure 5? [2]

Q 3.C.2) Write down the truth table for the logic function,
Y_1 = A'B'C' + AB'C'D' + A'B'C + ACD' + ABC'D + A'CD' + AB'CD'. [1]
From the truth table, draw the Karnaugh Map and then find the simplest form of the logic function for Y_1. [2]

Q 3.C.3) Repeat the question in (Q 3.C.2) with the additional condition that, for the input value-combinations of (A, B, C, D) = (1, 1, 0, 0), and (0, 1, 0, 1), the logic output of Y_1 is "Don't Care". Show the new truth-table and find the simplest form of the modified Y_1 using a new Karnaugh Map. [1] [2]

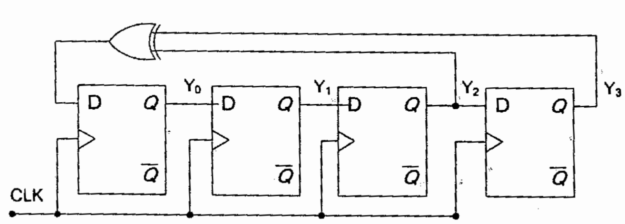

Figure 6. Digital Logic Circuit (Q 3.D)

For the circuit in Figure 6 plot CLK, Y_0, Y_1, Y_2, and Y_3 for from 0 ms to 4.5 ms. All D-FF's are positive edge-triggered.

Q 3.D) At time t = 0 ms, assume $Y_0 = Y_1 = Y_2$ = '0', Y_3 = '1' [4]