INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

Date ... 20 / 04 / 2012..... FN / AN Time : ~~2~~ / 3 Hrs. Full Marks ....60..... No. of Students ..... 102 .....

~~Autumn~~ / Spring Semester ..... Dept. ..... **E & ECE** ..... Sub. No. ..... **EC 31004** .....

... 3rd .... Yr. B. Tech. (H) / ~~B. Arch (H)~~ / ~~M. Sc.~~ Sub. Name ..... **VLSI Engineering** .....

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1. The final answers (numerical values with unit) should be underlined or enclosed in box.
2. For any value related to any device parameter or circuit parameter, which you may find not given with a problem, **assume a suitable value** for such parameter.
3. For each problem, write the answers of all its parts together and avoid writing answers of its various parts at different locations in your answer-script.

For all problems assume the following parameter values, unless explicitly specified for a particular problem.
V_{DD} = 2.5 V, the design rule λ = 125 nm. $(W/L)_{NMOS} = 8\lambda / 4\lambda$. $(W/L)_{PMOS} = 16\lambda / 4\lambda$.
Process trans-conductance parameter, $k_n' = 100$ uA / V^2, $k_p' = 50$ uA / V^2 ; Threshold voltage: $V_{Tn} = |V_{Tp}| = 0.2\ V_{DD}$,
Use channel length modulation parameter, $\lambda_n = \lambda_p \approx 0.1\ V^{-1}$ for small-signal analysis.
Ignore body-bias effect (i.e. $\gamma_n = \gamma_p \approx 0\ V^{0.5}$). Assume all the o/p node capacitances are lumped into the single capacitance, C_L, where C_L = 100 fF.

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1. Problem on MOS amplifier and switch: 0.5x24 = 12 points

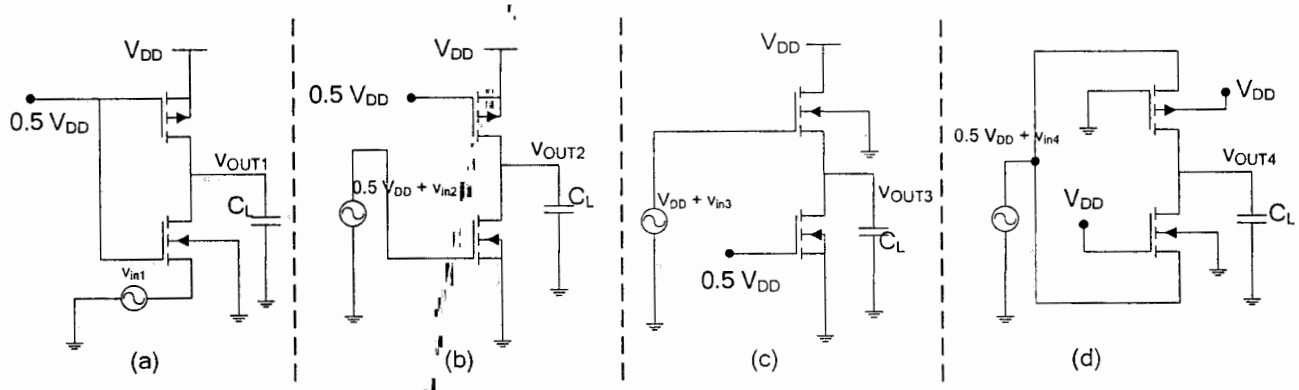

Figure 1. MOS Amplifier and Switch circuit

For the circuit in Figure 1(a):
(1.a.1) Find the DC values of I_D [uA] and V_{OUT} [V].
(1.a.2) Find the value of low-frequency small-signal voltage-gain, $A_v = v_{out} / v_{in}$ [V/V].
(1.a.3) Find the value of low-frequency small-signal output impedance, R_{out} [Ω].
(1.a.4) Find the value of low-frequency small-signal input impedance, R_{in} [Ω].
(1.a.5) Find the value of 3-dB band-width, ω_{3dB} [rad/s].
(1.a.6) Find the value of equivalent input noise spectral density, $\overline{v_{in,n}}^2$ [V^2/Hz].

For the circuit in Figure 1(b):	For the circuit in Figure 1(c):	For the circuit in Figure 1(d):
(1.b.1) Repeat (1.a.1).	(1.c.1) Repeat (1.a.1).	(1.d.1) Repeat (1.a.1).
(1.b.2) Repeat (1.a.2).	(1.c.2) Repeat (1.a.2).	(1.d.2) Repeat (1.a.2).
(1.b.3) Repeat (1.a.3).	(1.c.3) Repeat (1.a.3).	(1.d.3) Repeat (1.a.3).
(1.b.4) Repeat (1.a.4).	(1.c.4) Repeat (1.a.4).	(1.d.4) Repeat (1.a.4).
(1.b.5) Repeat (1.a.5).	(1.c.5) Repeat (1.a.5).	(1.d.5) Repeat (1.a.5).
(1.b.6) Repeat (1.a.6).	(1.c.6) Repeat (1.a.6).	(1.d.6) Repeat (1.a.6).

2. Problem on MOS device-geometry scaling: 1 x 24 = 24 points

Refer to the circuits in **Figure 1**(a) through **Figure 1**(d) in Problem 1. Now, we scale-down the device-sizes for all the transistors in all of the above circuits. Scaling factor = 2. (E.g. $W' = \frac{W}{2}$, $L' = \frac{L}{2}$ etc.) Calculate the corresponding scaling factor of all the circuit-performance parameters. Ignore short-channel effects.

Figure 1(b): Device sizes are scaled down under constant-voltage scaling paradigm. Calculate:
(2.a.1) Scaling factor for I_D and for V_{OUT}
(2.a.2) Scaling factor for A_v
(2.a.3) Scaling factor for R_{out}
(2.a.4) Scaling factor for R_{in}
(2.a.5) Scaling factor for ω_{3dB}. Assume $C_L' = \frac{C_L}{2}$
(2.a.6) Scaling factor for $\overline{v_{in,n}}^2$

Figure 1(b): Device sizes are scaled down under constant-field scaling paradigm. Calculate:
(2.b.1) Scaling factor for I_D and for V_{OUT}
(2.b.2) Scaling factor for A_v
(2.b.3) Scaling factor for R_{out}
(2.b.4) Scaling factor for R_{in}
(2.b.5) Scaling factor for ω_{3dB}. Assume $C_L' = \frac{C_L}{2}$
(2.b.6) Scaling factor for $\overline{v_{in,n}}^2$

Figure 1(c): Device sizes are scaled down for the same fabrication technology itself. Calculate:
(2.c.1) Scaling factor for I_D and for V_{OUT}
(2.c.2) Scaling factor for A_v
(2.c.3) Scaling factor for R_{out}
(2.c.4) Scaling factor for R_{in}
(2.c.5) Scaling factor for ω_{3dB}. Assume $C_L' = \frac{C_L}{2}$
(2.c.6) Scaling factor for $\overline{v_{in,n}}^2$

Figure 1(d): Device sizes are scaled down under constant-field scaling paradigm. Calculate:
(2.d.1) Scaling factor for I_D and for V_{OUT}
(2.d.2) Scaling factor for A_v
(2.d.3)Scaling factor for R_{out}
(2.d.4)Scaling factor for R_{in}
(2.d.5) Scaling factor for ω_{3dB}. Assume $C_L' = \frac{C_L}{2}$
(2.d.6) Scaling factor for $\overline{v_{in,n}}^2$

3. Problem on pass-FET and Transmission Gate: (2 + 2 + 2 + 2) x 3 = 24 points

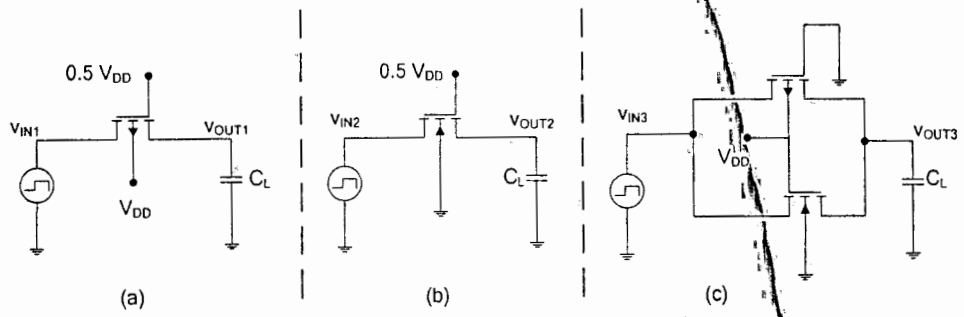

Figure 2. Pass Transistor and MOSFET switch circuit

In this problem, the notations used are:
V_{OH}: Output-high voltage; V_{OL}: Output-low voltage
$t_{LH}(x_1\%,y_1\%)$: the time taken for charging from x_1 % of output-voltage-swing to y_1 % of output-voltage-swing.
$t_{HL}(x_2\%,y_2\%)$: the time taken for discharging from x_2% of output-voltage-swing to y_2% of output-voltage-swing.
P_{dyn} : Dynamic power dissipation. Assume system-clock frequency, f_{CLK} = 10 MHz and switching activity factor, α = 1.
V_{IN}: Square-wave with peak-to-peak voltage-swing of 0V - V_{DD}.

Refer to Figure 2(a) circuit.
(3.a.1) V_{OH} = ? V_{OL} = ? [in V]
(3.a.2) t_{LH}(0%, 90%) = ? [in ps]
(3.a.3) t_{HL}(100%, 10%) = ? [in ps]
(3.a.4) P_{dyn} = ? [in uW]

Refer to Figure 2(b) circuit.
(3.b.1) V_{OH} = ? V_{OL} = ? [in V]
(3.b.2) t_{LH}(0%, 90%) = ? [in ps]
(3.b.3) t_{HL}(100%, 10%) = ? [in ps]
(3.b.4) P_{dyn} = ? [in uW]

Refer to Figure 2(c) circuit.
(3.c.1) V_{OH} = ? V_{OL} = ? [in V]
(3.c.2) t_{LH}(0%, 90%) = ? [in ps]
(3.c.3) t_{HL}(100%, 10%) = ? [in ps]
(3.c.4) P_{dyn} = ? [in uW]