Roll no: **Name:**

INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

Department of Computer Sc & Engg

Computer Organisation and Architecture (CS31001)

End-semester (Autumn)

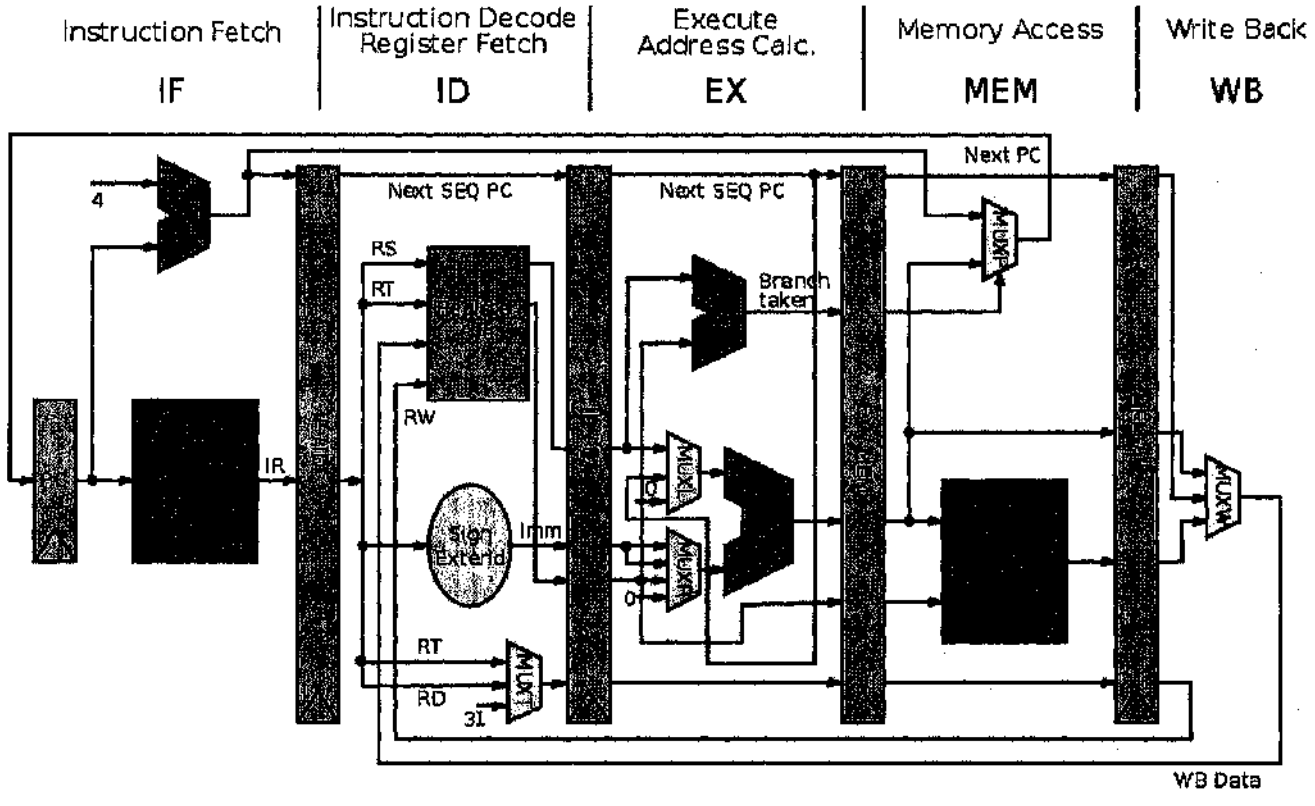
Place: F-116 *Date:* Fri, Nov 19, 2010 *Time:* 2-5pm (AN), 3 hours

Students: 80 *Marks:* 150

Answer ALL the questions.

Submit with the answerscript the page of question paper containing the diagram of CPU.

1. Study the CPU in the given figure and the given instructions along with their formats given below. In the given diagram, mark and label control points that are critical to its operation; also label the inputs to `MUXT`. 6+2



For each of the instructions listed below with their instruction formats, do the following: (*i*) indicate the micro-instructions along with activation of control signals (as labelled earlier) that need to be carried out in each pipeline stage and (*ii*) indicate the information (both control and data) that must be stored in the inter-pipeline stages for proper execution of the instruction.

(a) The `sub rs, rt, rd` instruction for calculating the the difference between `rs` and `rt` and saving the result in `rd`.

bits	31:26	25:21	20:16	15:11	10:6	5:0
name	op	rs	rt	rd	shamt	funct

5+4

CM×83498

(b) The `lw rt, (imm)rs` instruction for transferring the contents of `M[imm+rs]` to `rt`.

bits	31:26	25:21	20:16	15:0
name	op	rs	rt	imm

5+4

(c) The `bne rs, rt, disp` instruction for branching to `PC+4`$\times$`disp` if `rs`$\neq$`rt`.

bits	31:26	25:21	20:16	15:0
name	op	rs	rt	disp

5+4

(d) Discuss the implications of moving `MUXP` to the `EX` stage. 5

2. (a) Develop the expression for asymtotic speed up of a p-stage pipelined processor, assuming that the delay of stage-i is T_i. Also, state any assumptions for the derivation. 5

(b) Discuss data hazards in a pipelined CPU. How are these hazards mitigated? 6

(c) Discuss control hazards in a pipelined CPU. How are these hazards mitigated? 6

(d) Discuss the contraction of the five stage pipeline to a four stage pipeline. 3

3. (a) Depict the steps for multiplying -5×-2 using the shift-and-add multiplication algorithm. 6

(b) Explain the need of the end correction when multiplying with a negative multiplier using the shift-and-add multiplication algorithm. 5

(c) Depict the steps for multiplying -5×-2 using the (radix-2) Booth's multiplication algorithm. 6

(d) Explain why the end correction is not needed with the Booth's multiplication algorithm? 5

(e) Giving detailed explanations, derive the decision table for the radix-4 Booth's multiplication algorithm. 8

4. (a) Depict the division of 57 by 6 using restoring division. 5

(b) Outline the steps for non-restoring division and justify the correctness of the technique. 5+5

(c) Develop the data paths for a non-restoring array divider for positive numbers; also give the organisation of the CAS cell. 5+5

(d) Outline the steps for radix-2 SRT division, given a justification for its convergence. 7+3

(e) Explain the procedure for converting balanced signed digit to regular binary. 5

(f) Present a combinational circuit to convert from balanced signed digit to regular binary. 5

5. (a) Give an example to illustrate that floating point addition is not associative. 4

(b) Outline the steps for floating point addition in a flowchart form. 6

(c) Describe the use of *guard*, *round* and *sticky* bits for improving accuracy in floating point computations. 5